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Attorney Docket No.	P04659
First Inventor or Application Identifier	Herring et al.
Title	DECT-Like System And Method Of Transceiving Information Over The Industrial-Scientific-Medical Spectrum
Express Mail Label No.	EK232118678US

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APPLICATION ELEMENTS
See MPEP chapter 600 concerning utility patent application contents.

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1. [X] * Fee Transmittal Form (e.g., PTO/SB/17) (Submit an original and a duplicate for fee processing)
2. [X] Specification [Total Pages 105] (preferred arrangement set forth below)
   - Descriptive title of the Invention
   - Cross References to Related Applications
   - Statement Regarding Fed sponsored R & D
   - Reference to Microfiche Appendix
   - Background of the Invention
   - Brief Summary of the Invention
   - Brief Description of the Drawings (if filed)
   - Detailed Description
   - Claim(s)
   - Abstract of the Disclosure
3. [X] Drawing(s) (35 U.S.C. 113) [Total Sheets 6]
4. Oath or Declaration [Total Pages]
   a. [ ] Newly executed (original or copy)
   b. [ ] Copy from a prior application (37 C.F.R. § 1.63(d)) (for continuation/divisional with Box 16 completed)
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5. [ ] Microfiche Computer Program (Appendix)
6. Nucleotide and/or Amino Acid Sequence Submission (if applicable, all necessary)
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ACCOMPANYING APPLICATION PARTS

7. [ ] Assignment Papers (cover sheet & document(s))
8. [ ] 37 C.F.R.§3.73(b) Statement (when there is an assignee) [ ] Power of Attorney
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5. 6 sheets of drawings
6. Declaration of ____ inventor(s) (x) Unsigned
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DECT-Like System and Method Of Transceiving Information Over The Industrial-Scientific-Medical Spectrum

Cross Reference To Related Applications

This application is related to commonly assigned and co-pending US patent application serial number 09/xxx,xxx (attorney's docket number P04658) entitled "System And Method For Concurrent Wireless Voice And Data Communications" contemporaneously filed herewith and herein incorporated by reference.

Background of the Invention

1. Field of the Invention:

The invention relates generally to wireless communications and more specifically to a system and method employing standard DECT hardware to operate in the Industrial-Scientific-Medical (ISM) band.

2. Description of Related Art:

The following background information is provided to aid in the understanding of the application of the present invention and is not meant to be limiting to the specific examples set forth herein. The so-called "Industrial-Scientific-Medical (ISM)" band allows for unlicensed wireless operation in the 2.4 GHz spectrum (as well as the 900MHz and 5.8 GHz spectrum) provided however, that the power output is less than one watt and that some form of spread spectrum technology, i.e. Frequency Hopping Spread Spectrum (FHSS), Direct Sequence Spread Spectrum (DSSS) or a hybrid of FHSS and DSSS, is used to minimize interference. In the United States, 47 CFR Part 15 specifies the use of at least seventy-five (75) hopping frequencies between 2.4 GHz and 2.4835 GHz and a minimum hop rate of 2.5 hops per second for FHSS systems. Several schemes have been proposed to use the ISM spectrum for wireless data

communication applications, such as for Wireless Local Area Networks (WLANs).

In its 802.11 standard, the IEEE promulgated, inter alia, FHSS and DSSS definitions for the physical layer of a WLAN. For FHSS in North America and most of Europe, IEEE 802.11 requires 79 channels in 1 MHz steps beginning at 2.402 GHz and ending at 2.480 GHz with a minimum frequency hop of 6 MHz. Fig. 8 depicts the IEEE 802.11 protocol for packetizing information in a FHSS WLAN. One-hundred-twenty-eight (128) bits (a 96 bit preamble and 32 bit header) are sent to assist in synchronizing after a carrier hops from one frequency to the next. Payload data then follows in sizes ranging from 1 to 4095 bytes.

An example of an ISM FHSS WLAN is the HomeCast™ Open Protocol (HOP™) from Alation Systems Inc. of Mountain View, California embodied in one form as the HomeFree™ Wireless Network product from Diamond Multimedia Systems, Inc. of Vancouver, Washington. The HOP system provides 79 channels and a maximum data throughput of 1 Mbps but employs a proprietary ISM baseband processor, requires a host processor to implement a software MAC, and does not support voice communications.

The so-called "PRISM I" chipset from the Intersil Corporation of Melbourne, Florida, is an example of a DSSS WLAN implementation in compliance with the IEEE 802.11 standard. The PRISM I chipset comprises six discrete integrated circuits, requires a proprietary baseband processor, and while maintaining IEEE 802.11 compliant, can only achieve a maximum data throughput of 2 Mbps and does not support voice communications. It can be seen therefore, that the PRISM I DSSS solution while improving data throughput, also increases chip count and cost and locks the design into proprietary hardware.

By way of further background, reference is made to Fig. 1 that depicts the prior art Digital Enhanced Cordless Telecommunications (DECT) standard protocol promulgated by the European Telecommunications Standards Institute (ESTI). The DECT standard defines a Multiple Carrier, Time-Division-Multiple-Access (TDMA), Time-Division-Duplex (TDD) protocol with ten channels (carrier frequencies) between 1881.792 MHz and 1897.344 MHz spaced 1.728 MHz apart. Each of the ten channels supports a ten-millisecond frame comprised of twenty-four time slots. TDD is provided by allocating twelve of the twenty-four slots for base station to cordless handset communications and the other twelve slots for cordless handset to base station communications. Each time slot comprises 480 bits with a 32-bit preamble for synchronization, 388 bits for data and 60 bits for guard time. The 388 data bits are further divided into an A-field, a B-field and 4 parity bits for error detection. The A-field comprises an 8-bit header, 40 bits of control information and 16 cyclic redundancy check (CRC) bits while the B-field provides 320 bits of data.

For speech applications, analog signals are digitized and encoded using adaptive differential pulse code modulation (ADPCM). Frequency hopping is employed to avoid interference by periodically assigning a different one of the ten channel frequencies to each of the twenty-four time slots. A form of frequency shift keying known as Gaussian filtered, minimum shift keying (GMSK) is used to modulate the transmitted signal to provide continuous phase transitions between two adjacent symbols.

DECT enabled products are ubiquitous in Europe ranging from telephones and WLANs to cordless terminal mobility (CTM) applications wherein a cordless handset operates with both private and public base stations. Unfortunately in the United States as well in other countries, the DECT spectrum between 1881.792 MHz and 1897.344 MHz is licensed for Personal Access

Communication Systems (PACS) and is not available for unlicensed applications such as WLANS.

From the foregoing it can be seen that there is a need for a system and method employing standard DECT hardware but operates in the unlicensed Industrial-Scientific-Medical (ISM) spectrum.

Summary of the Invention

To overcome the limitations of the prior art described above, and to overcome other limitations that will become apparent upon reading and understanding the present specification, the present invention discloses a system and method employing standard DECT hardware adapted for use in the Industrial-Scientific-Medical (ISM) Spectrum. A Frequency Hopping Spread Spectrum (FHSS), multiple carrier, time-division-multiple-access (TDMA), time-division-duplex (TDD) technique provides wireless communications over the ISM Spectrum while employing standard DECT hardware to map and morph the DECT protocol to operate within the ISM spectrum. A baseband processor provides, among other things, slot and frame timing to a RF sub-module. The preferred, although not exclusive number of carrier frequencies is programmed to seventy-five ranging between 2401.122 MHz to 2479.813 MHz and spaced 1.063 MHz apart. Each of the seventy-five channels supports a ten-millisecond frame preferably although not exclusively comprised of sixteen time slots. TDD is provided by allocating half of the slots for first to second tranceiving unit communications and the other half for second to first tranceiving unit communications.

A feature of the present invention is that standard hardware may be employed for either DECT or ISM applications.

These and various other objects, features, and advantages of novelty which characterize the invention are pointed out with particularity in the claims

annexed hereto and forming a part hereof. However, for a better understanding of the invention, its advantages, and the objects obtained by its use, reference should be made to the drawings which form a further part hereof, and to the accompanying descriptive matter, in which there is illustrated and described a specific example of DECT-Like System and Method of Transceiving Information Over The Industrial-Scientific-Medical Spectrum in accordance with the principles of the present invention.

Brief Description of the Drawings

Fig. 1 depicts a prior art diagram of the Digital Enhanced Cordless Telecommunications (DECT) standard protocol promulgated by the European Telecommunications Standards Institute (ESTI);

Fig. 2 depicts an illustrative but not limiting block diagram of a concurrent wireless voice and data communications system practiced in accordance with the principles of the present invention;

Fig. 3 depicts an illustrative but not limiting block diagram of a preferred Personal Access Device (PAD) practiced in accordance with the principles of the present invention;

Fig. 4 depicts a first exemplary but not limiting block diagram of a first preferred base station practiced in accordance with the principles of the present invention;

Fig. 5 depicts a second exemplary but not limiting block diagram of a second preferred base station practiced in accordance with the principles of the present invention;

Fig. 6 depicts an exemplary but not limiting block diagram of a preferred transceiver module practiced in accordance with the principles of the present invention;

Fig. 7 depicts the preferred protocol for a concurrent wireless voice and data communications system practiced in accordance with the principles of the present invention;

Fig. 8 depicts the preferred TDMA protocol for a concurrent wireless voice and data communications system practiced in accordance with the principles of the present invention, and,

Fig. 9 depicts a prior art IEEE 802.11 protocol for packetizing information in a frequency hopping spread spectrum wireless local area network.

Description of the Preferred Embodiment

The detailed description of the preferred embodiment for the present invention is organized as follows:

This organizational table and the corresponding headings used in this detailed description are provided for the convenience of reference only and are not intended to limit the scope of the present invention. It is to be understood that while the preferred embodiment is described herein below with respect to DECT and DECT-like wireless protocols, it has general applicability to any digital wireless communications technology. Certain terminology known to practitioners in the field of wireless communications is not discussed in detail in order not to obscure the disclosure. Moreover, in order not to obscure the disclosure with structural details which will be readily apparent to those skilled in the art having the benefit of the description herein, the structure, control and arrangement of conventional circuits have been illustrated in the drawings by readily understandable block representations showing and describing details that are pertinent to the present invention. Thus, the block diagram illustrations in the figures do not necessarily represent the physical arrangement of the exemplary system, but are primarily intended to illustrate the major structural components in a convenient functional grouping, wherein the present invention may be more readily understood.

Reference is now made to the accompanying drawings, which form a part hereof, and in which is shown by way of illustration specific embodiments in which the invention may be practiced. It is to be understood that other

embodiments may be utilized and structural changes may be made without departing from the scope of the present invention.

1.0 Exemplary System

Reference is now made to Fig. 2 that depicts an illustrative but not limiting block diagram of a concurrent wireless voice and data communications system practiced in accordance with the principles of the present invention. A Personal Access Device (PAD) 100 and base station 102 employ the present invention to provide RF connectivity therebetween. The PAD 100 preferably resides in a charging cradle 104 to keep rechargeable batteries (not shown) refreshed when not in use. When the PAD 100 is stationary and docked on the charging cradle 104, commands may be entered with an optional keyboard 108 such as through the USB port 117. When the PAD 100 is mobile, commands may be entered on the touch screen/touch keyboard (described in more detail herein below) of the PAD 100 with a detachable stylus 106 that resides within a storage cavity formed in case of the PAD 100. The PAD 100 includes a microphone and speakers (described below) to support full duplex phone communications.

The base station 102 may manifest itself as an advanced set-top box 102a coupled to a television-like monitor (not shown), a stand-alone personal computer 102b or as a low cost stand alone device 102c with no display. The base station 102 is tethered to a voice network 109 that may manifest itself as but is not limited to a PSTN, and to a data network 110 that may manifest itself as but is not limited to, an Ethernet adapter, CATV, XDSL, ISDN or V.90 modems.

2.0 Exemplary Personal Access Device (PAD)

Reference is now made to Fig. 3 that depicts an illustrative but not limiting block diagram of a preferred PAD 100 practiced in accordance with the principles of the present invention. A highly integrated processor 112 such as but not limited to, the Geode™ family of processors from National

Semiconductor Corporation, Santa Clara, California, is coupled to DRAM 114 through an integrated DRAM controller (not shown) in the processor 112. A so-called "south bridge" chipset 116 is coupled to the processor 112, preferably through a PCI bus 113. The south bridge chipset 116 preferably includes an integrated ISA bus controller coupled to an ISA bus 115, a USB port 117 for supporting, inter alia, the keyboard 108 and FIFO buffers coupled to an audio CODEC 118. A flash ROM 111 is connected to the ISA bus 115 for storing code (such as an operating system and application programs) that is shadowed into DRAM 114 for execution by processor 112. The audio CODEC 118 converts digital signals to analog signals and drives speakers 121 and receives and converts analog signals from a monaural microphone 123 to digital signals for processing by processor 112. The display 120, which preferably is a DSTN or TFT LCD, is refreshed by a display adapter (not shown) that is integrated into either the processor 112 or chipset 116. The display 120 includes an overlaid programmable touch control panel 101 controlled by microcontroller 127 for use with removable stylus 106. The microcontroller 127 also provides charge profiling for rechargeable battery 129. The transceiver module 125 (discussed in more detail hereinbelow) is preferably, although not exclusively, connected to the ISA bus 115 for providing a wireless link to the base station 102.

3.0 Exemplary Base Station

Reference is now made to Fig. 4 that depicts a block diagram of the first preferred base station 102 without the transceiver module 125 installed, practiced in accordance with the principles of the present invention. While the first exemplary embodiment of the base station 102 is depicted as having a V.90 modem 135, those skilled in the art will readily recognize with the aid of the present disclosure, other forms of data network interfaces including but not limited to, ISDN, DSL and CATV modems and network adapters such as, but not limited to, Ethernet without departing from the scope of the present invention.

The V.90 modem interface 135 of the base station 102 is coupled to a Public switched telephone network (PSTN) through RJ11 jack 130. RJ11 jack 130 connects a first analog phone line through a first Digital Access Arrangement (DAA) 131 included within the V.90 modem 135. A combined CODEC/hybrid circuit 136 separates transmitted signals from received signals from the PSTN and converts the received signals into digital form. The received digital signals are operated on by a digital signal processor (DSP) 138 that executes code out of flash ROM 140 and SRAM 142 and 144 to provide, inter alia, interface control, AT command processing, and processing functions needed to perform signal modulations. Through execution of the code, the DSP 138 provides a command line AT interpreter, error checking, re-transmission, compression and decompression functions as well as necessary signal modulation/demodulation, adaptive filtering and encoding/decoding required for a V.90 standard modem.

A second RJ11 jack 132 connects a second analog phone line from the PSTN to a second DAA 133 for voice reception/transmission. An optional third RJ11 jack 134 may be used to connect an external handset (not shown) to the base station 102. Optional LED indicators 143 controlled by DSP 138 display status of device ready, data and voice transmission in progress. Optional page key 145 may be provided to signal the transceiver module 150 (depicted in Fig. 5) through connector 149a to emit a page signal to the PAD 100. A power on reset (POR) circuit 147 provides reset signals to circuitry on the base station 102 as well as through connector 149a to the transceiver module 125, described in more detail herein below.

Reference is now made to Fig. 5 that depicts a block diagram of a second preferred base station 102′ without the transceiver module 125 installed, practiced in accordance with the principles of the present invention. The second preferred base station 102′ is constructed similar to that of the first base station 102 except for the elimination of secondary DAA 133 and the addition of the

relay 137. In the second preferred version of the base station 102', relay 137, which is controlled via the baseband processor 180 in transceiver module 125, switches the PSTN coupled through RJ11 jack 130 and DAA 131 to either the data network adapter (e.g. modem) or the ancillary analog voice channel (provided by the baseband processor 180 in transceiver module 125), all of which is discussed in more detail herein below.

Although while only one phone line is connected to the base station 102', the user of a PAD 100 can utilize the data network (via modem) and still be made aware of an incoming call via the transceiver module 125 that provides call notification and caller ID to allow the user of the PAD 100 to switch from the data network to the voice network. For example, this may manifest itself through a pop-up window on the PAD 100 notifying a single phone line user of PAD 100 (who may be surfing the world-wide-web) of an incoming phone call thus permitting the user of PAD 100 to switch from surfing the web to answer the phone call.

4.0 Exemplary Transceiver Module

Reference is now made to Fig. 6 that depicts by way of illustration an exemplary but not limiting block diagram of the preferred transceiver module 125 practiced in accordance with the principles of the present invention. The transceiver module 125 comprises an antenna 152 (multiple antennas for diversity), an RF sub-module 150 coupled to a baseband processor 180, a flash ROM 182 and RAM 183 to store code for execution by the baseband processor 180 and a mating connector 149b for connecting to either the base station connector 149a or to the ISA bus 115 in the PAD 100.

The RF sub-module 150 includes, inter alia, a band pass filter (BPF) 154 coupled to a transmit/receive switch 156. Received data from the transmit/receive switch 156 is conditioned by a low noise amplifier (LNA) 158

and a BPF 160 prior to being sent to a mixer within single chip radio transceiver 162. Transmitted data from the single chip radio transceiver 162 is passed through a LNA 164 and transmit power amplifier 166 prior to being sent to transmit/receive switch 156. An exemplary but not limiting example of a single chip containing the BPFs 154 and 160, LNAs 158 and 164, transmit/receive switch 156 and power amplifier 166 is the AU2404T RF front-end integrated circuit from Alation Systems Inc. of Mountain View, California. Those skilled in the art, with the aid of the present disclosure, will recognize other forms and solutions for elements 154, 156, 158, 160, 164 and 166 without departing from the spirit and scope of the present invention.

The single chip radio transceiver 162 in combination with BPFs 168 and 170 and voltage controlled oscillator (VCO) 172 and loop filter 174 down convert (receive) or up convert (transmit) data to/from baseband processor 180. The preferred although not exclusive embodiment for the single chip radio transceiver 162 is the LMX3162 transceiver from National Semiconductor Corporation of Santa Clara, CA, described in the National Analog and Interface Products Databook (and accompanying CD-ROM), 1999, which is herein incorporated by reference. The RF sub-module 150 is available from ALPS Electric Co, Ltd. of Tokyo, Japan under the model numbers UGSA4-402A (without antenna diversity) and UGSA4-502A (with antenna diversity) for 2.4 GHz operation and under the model numbers UGSE2-402A (without antenna diversity) and UGSE2-502A (with antenna diversity) for 1.8 GHz (DECT) operation.

The baseband processor 180 preferably comprises a CODEC and at least one sub-processor that executes code stored in flash ROM 182 and RAM 183 to handle, inter alia, audio, signal and data processing for tone generation, echo canceling and to program slot and frame timing for the RF sub-module 150. In general, the code executed by the baseband processor 180 in the transceiver

module 125 is preferably layered in adherence with the Open Systems Interconnection (OSI) model, the details of which are known to one skilled in the art. The preferred although not exclusive embodiment for the baseband processor 180 is the SC14424 baseband processor from National Semiconductor Corporation of Santa Clara, CA, described in detail in Appendix A hereto.

Reference is now made to Fig. 7 that depicts the preferred protocol for a concurrent wireless voice and data communications system practiced in accordance with the principles of the present invention. The preferred protocol is a multiple carrier, Time-division-multiple-access (TDMA), Time-division-duplex (TDD) system. The preferred programmable, although not exclusive number of carrier frequencies is seventy-five ranging between 2401.122 MHz to 2479.813 MHz and spaced 1.063 MHz apart. Those skilled in the art having the benefit of the description herein will appreciate other numbers of carrier frequencies (e.g. ten), frequency spectrums (e.g. 1881.792 MHz to 1897.344 MHz) and spacings (e.g. 1.728 MHz apart) without departing from the scope the present invention. Each of the seventy-five channels supports a ten-millisecond frame preferably comprised of sixteen time slots. Those skilled in the art having the benefit of the description herein will appreciate other numbers of time slots without departing from the scope the present invention. Symmetrical TDD is provided by allocating half (i.e. eight of the sixteen slots) for base station to PAD communications and the other half (i.e. eight slots) for PAD to base station communications. Asymmetrical TDD is contemplated as well wherein base station to PAD communications consume more slots (e.g. twelve slots) than PAD to base station communications (i.e. four slots) or vice versa. Those skilled in the art having the benefit of the description herein will appreciate other asymmetric numbers of slot allocations for base station to PAD communications and vice versa without departing from the scope the present invention.

Each time slot preferably comprises a 32-bit preamble for synchronization, a 64 bit A-field for signaling and a B-field comprising 320 bits and 4 bits for CRC. Each of the sixteen time slots receives/transmits on one of the seventy-five carrier channels that preferably changes in a pseudo-random fashion, to one of the other seventy-four carrier channels after two consecutive frames thus providing fifty (50) hops/second. Those skilled in the art having the benefit of the description herein will appreciate other number of frequency carriers, hopping patterns and frequency hop periods without departing from the scope the present invention.

Reference is now made to Fig. 8 that depicts the preferred TDMA protocol in more detail. In the preferred embodiment, symmetric TDMA (with respect to both voice/data and base station/PAD communications) is provided by allocating time slots 1, 2, 3 and 9, 10, 11 for data communication between base station and PAD and PAD and base station, respectively, and time slots 4, 5, 6 and 12, 13, 14 for voice communication between base station and PAD and PAD and base station, respectively. Time slots 7 and 15 are reserved, time slot 8 is allocated to program the transmit carrier frequency in the single chip radio transceiver 162 and slot 16 is allocated to program the receive carrier frequency.

Asymmetrical TDMA is contemplated as well wherein data communications consume more slots (e.g. twelve slots) than voice communications (i.e. four slots) or vice versa. As mentioned above, asymmetry with respect to base station/PAD communications is contemplated and it is further contemplated that asymmetric base station/PAD communications may be used in combination with asymmetric data/voice TDMA. Those skilled in the art having the benefit of the description herein will appreciate other asymmetric numbers of slot allocations for base station/PAD communications and/or data/voice communications without departing from the scope the present invention.

To achieve frequency hopping, the transmit and receive carrier frequencies are changed by the baseband processor 180 reprogramming a phase locked loop (PLL) in the single chip radio transceiver 162. The transmit and receive carrier frequencies are changed by the baseband processor 180 in a pseudo-random fashion, to one of the other seventy-four carrier channels after two consecutive frames thus providing fifty (50) hops/second.

Referring to Fig. 8b, a time slot dedicated to data allocates 80 bits in the B field to a Forward Error Correction Code (FECC). The remaining 240 bits are payload data for processing by the PAD 100. A time slot dedicated to voice allocates the entire 320 bits in the B field to voice information since voice is tolerant to dropouts in bit patterns.

So-called "multi-slot" operation (e.g. double slot) is further contemplated wherein adjacent slots share a single set of sync, signaling, CRC bits and optionally, FECC bits. In a single data slot, the sync, signaling, CRC and FECC bits consume 180 out of the 420 bits allocated to a slot. By way of illustration and not of limitation, a double data slot shares one 32-bit preamble for synchronization, one 64 bit A-field for signaling, one set of 80 FECC bits and one set of four CRC bits, thus providing 660 payload data bits over two slots instead of the standard 480 bits – a 37.5% increase in bandwidth. Those skilled in the art having the benefit of the description herein will appreciate other multi-slot configurations (e.g. quad slots) and allocation of overhead bits without departing from the scope the present invention.

5.0 PAD to Base Station Synchronization

On power up, the baseband processor 180 in the transceiver module 125 of the PAD 100 executes code to set the received carrier frequency to a reference channel and to scan for incoming data during a time period of two frames (e.g. 20 milliseconds). If an A-Field with a correct CRC is detected, the baseband

processor 180 continues to sample and decode A-Fields every frame (e.g. 10 milliseconds) for the expected ID of the base station 102. If a timeout occurs, the baseband processor 180 code restarts with the next carrier frequency channel. If the correct ID for the base station 102 is received, the A-field decoding continues until the current slot number, frame number, multi-frame number, and carrier channel in which the base station 102 is scanning are received. The base band processor 180 updates its corresponding internal variables and enters into a locked state when this information is received.

The baseband processor 180 in the transceiver module 125 of the base station 102 executes code to fix the transmit carrier frequency to a reference channel until the PAD 100 synchronizes. Thereafter, the baseband processor 180 executes code to change the transmit carrier frequency in the transceiver module 125 of the base station 102 every two frames (e.g. 20 milliseconds) in a pseudo-random sequence so long as correct A-Fields are found in two consecutive frames. The PAD 100 continues to receive A-Fields until the expected ID of the base station 102 is received or a timeout occurs. If a timeout occurs, the process is restarted with the reference channel frequency.

6.0 PAD-to-PAD Communications

PAD-to-PAD communications is further contemplated wherein multiple PADs communicate with one another through a common base station 102. By way of illustration and not of limitation, a second PAD 100′ is added to Fig. 2 wherein PADs 100 and 100′ communicate with one another via the base station 102. Each PAD 100 and base station have a unique ID associated with it that can be embedded in the A-field (64 bits of signaling) of the intended target. The baseband processor 180 in the transceiving module 125 of the base station 102 detects whether the received ID in the A-field is intended for the base station 102. If so, the voice/data information associated with that A-field is processed and routed to the respective voice/data network tethered to the base station 102. If

not, the base station 102 relays the voice/data information associated with that A-field onto the intended PAD 100′.

7.0 Conclusion

Although the Detailed Description of the invention has been directed to certain exemplary embodiments, various modifications of these embodiments, as well as alternative embodiments, will be suggested to those skilled in the art. The invention encompasses any modifications or alternative embodiments that fall within the scope of the Claims.

WHAT IS CLAIMED IS:

1. A transceiving unit for wireless communications over the industrial-scientific-medical (ISM) spectrum comprising:

(a) an RF sub-module for transceiving information in a 2.4 to 2.5 GHz band; and,

(b) a DECT baseband processor coupled and adapted to provide time slot and frame timing to the RF sub-module such that at least seventy-five hopping frequencies between 2.4 GHz and 2.4835 GHz and a minimum hop rate of 2.5 hops per second are maintained.

2. The transceiving unit as recited in claim 1 wherein the baseband processor comprises first and second means for supporting concurrent voice and data communications.

3. The transceiving unit as recited in claim 1 wherein each time slot comprises a 32-bit preamble for synchronization, a 64 bit A-field for signaling and a B-field comprising 320 bits and 4 bits for CRC.

4. The transceiving unit as recited in claim 1 wherein the baseband processor provides time slot and frame timing such that the at least seventy-five carrier frequencies are programmed ranging between 2401.122 MHz to 2479.813 MHz and spaced 1.063 MHz apart.

5. The transceiving unit as recited in claim 4 wherein the baseband processor provides time slot and frame timing such that each of the at least seventy-five channels supports a ten-millisecond frame.

6. The transceiving unit as recited in claim 5 wherein the baseband processor provides time slot and frame timing such that each frame comprises sixteen time slots.

7. The transceiving unit as recited in claim 6 wherein the sixteen time slots preferably change carrier channels after two consecutive frames.

8. The transceiving unit as recited in claim 7 wherein unequal amounts of time slots are allocated between voice and data communications.

9. The transceiving unit as recited in claim 7 wherein time slots 1, 2, 3 and 9, 10, 11 are allocated for data communication and time slots 4, 5, 6 and 12, 13, 14 are allocated for voice communications.

10. The transceiving unit as recited in claim 9 wherein time slot 8 is allocated to program the transmit carrier frequency and slot 16 is allocated to program the receive carrier frequency.

11. The transceiving unit as recited in claim 9 wherein time slots 1, 2, 3 and 9, 10, 11 allocate 80 bits in the B field to a Forward Error Correction Code (FECC).

12. The transceiving unit as recited in claim 9 wherein time slots time slots 4, 5, 6 and 12, 13, 14 allocate the entire B field to voice information.

13. A wireless communications method over the industrial-scientific-medical (ISM) spectrum comprising the steps of:

(a) transceiving information in a 2.4 to 2.5 GHz band; and,

(b) adapting a DECT baseband processor to provide time slot and frame timing for step (a) such that at least seventy-five hopping frequencies between 2.4 GHz and 2.4835 GHz and a minimum hop rate of 2.5 hops per second are maintained.

14. The method as recited in claim 13 wherein step (a) further comprises the step of supporting concurrent voice and data information.

15. The method as recited in claim 14 wherein the voice and data information are packetized into plural time slots within a time frame and share equal amounts of the time frame.

16. The method as recited in claim 15 wherein each of the plural time slots has a different one of the plural frequency channels.

17. The method as recited in claim 16 wherein each of the plural time slots changes to a different one of the plural frequency channels after a predetermined number of consecutive frames.

18. The method as recited in claim 16 further comprising the step of providing time slot and frame timing such that seventy-five carrier frequencies are programmed ranging between 2401.122 MHz to 2479.813 MHz and spaced 1.063 MHz apart.

19. The method as recited in claim 18 further comprising the step of providing time slot and frame timing such that each of the seventy-five channels supports a ten-millisecond frame.

20. A system for wireless communications over the industrial-scientific-medical spectrum comprising:

(a) a base station unit having a first transceiving unit;

(b) a cordless personal access device having a second transceiving unit; and,

(c) the first and second transceiving units including:

(i) an RF sub-module for transceiving information in a 2.4 to 2.5 GHz band; and,

(ii) a DECT baseband processor coupled and adapted to provide time slot and frame timing to the RF sub-module such that at least seventy-five hopping frequencies between 2.4 GHz and 2.4835 GHz and a minimum hop rate of 2.5 hops per second are maintained.

Abstract of the Disclosure

A system and method employs standard DECT hardware adapted for use in the Industrial-Scientific-Medical (ISM) Spectrum wherein a Frequency Hopping Spread Spectrum (FHSS), multiple carrier, time-division-multiple-access (TDMA), time-division-duplex (TDD) technique provides wireless communications over the ISM Spectrum while employing standard DECT hardware. A baseband processor provides slot and frame timing to a RF sub-module wherein the preferred, although not exclusive number of carrier frequencies is programmed to seventy-five ranging between 2401.122 MHz to 2479.813 MHz and spaced 1.063 MHz apart and wherein each of the seventy-five channels supports a ten-millisecond frame preferably, although not exclusively, comprised of sixteen time slots.

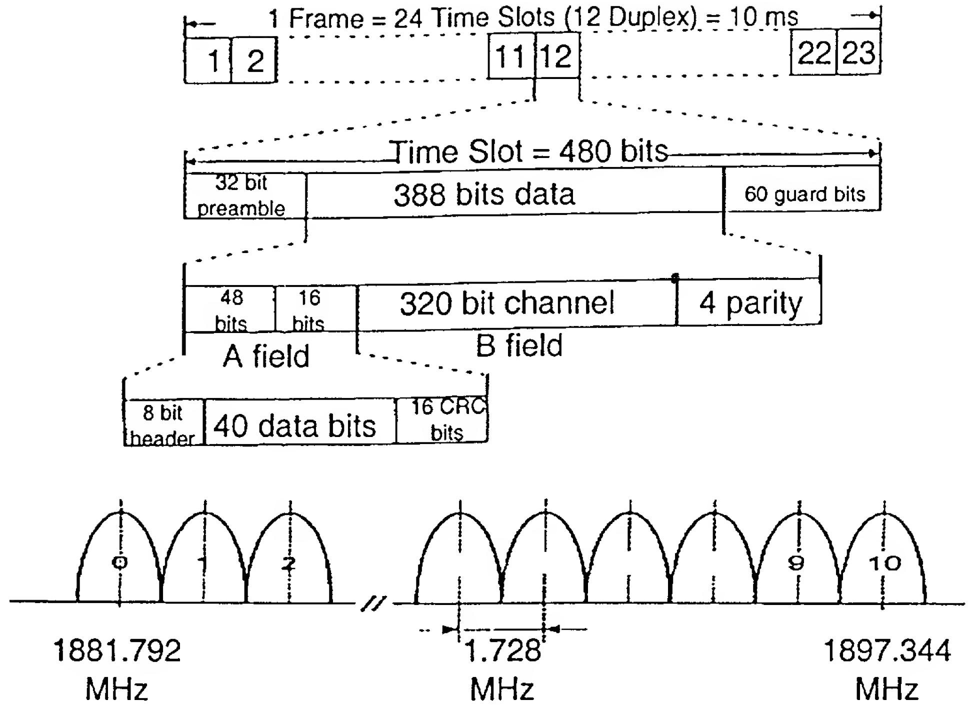


Fig. 1
(Prior Art)

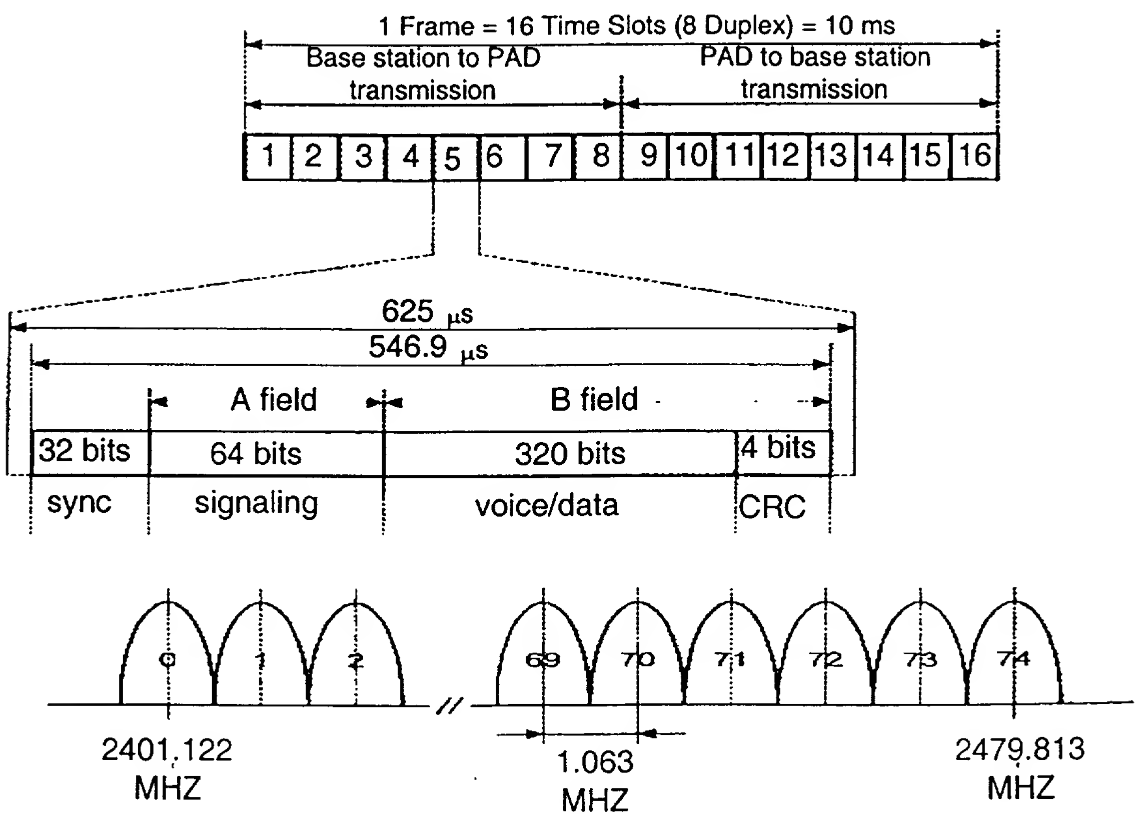


Fig. 7

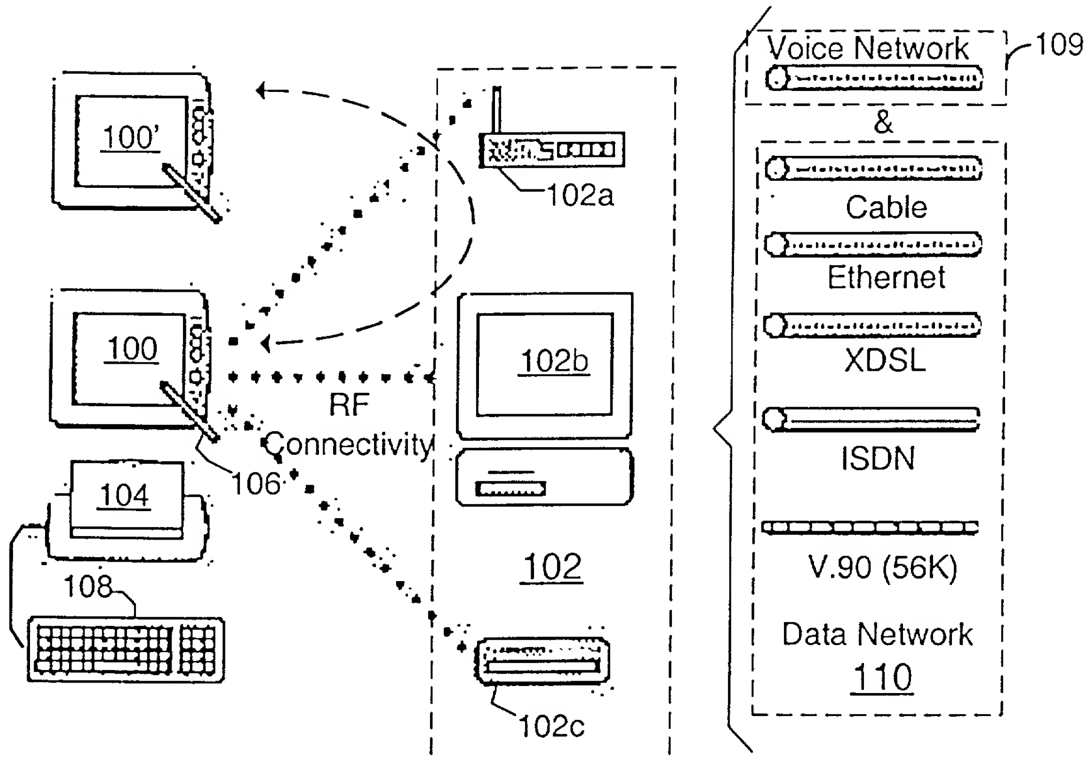

Voice Network
109
&
Cable
Ethernet
XDSL
ISDN
V.90 (56K)
Data Network
110
100'
102a
100
102b
RF
Connectivity
106
104
102
108
102c

Fig. 2

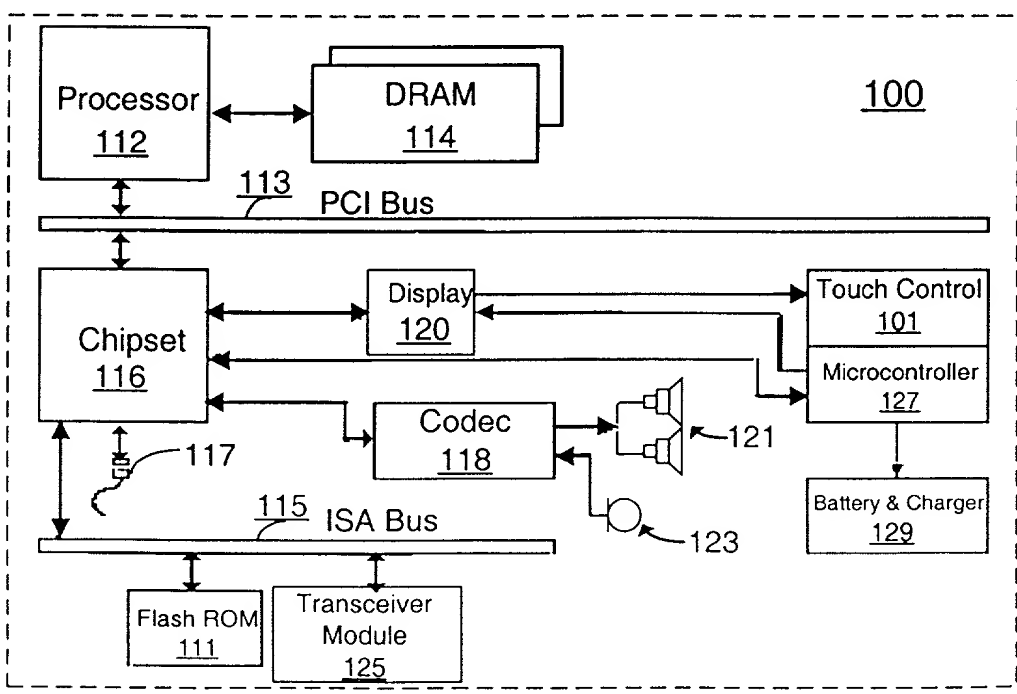

Processor
112
DRAM
114
100
113
PCI Bus
Chipset
116
Display
120
Touch Control
101
Microcontroller
127
Codec
118
121
117
Battery & Charger
129
115
ISA Bus
123
Flash ROM
111
Transceiver
Module
125

Fig. 3

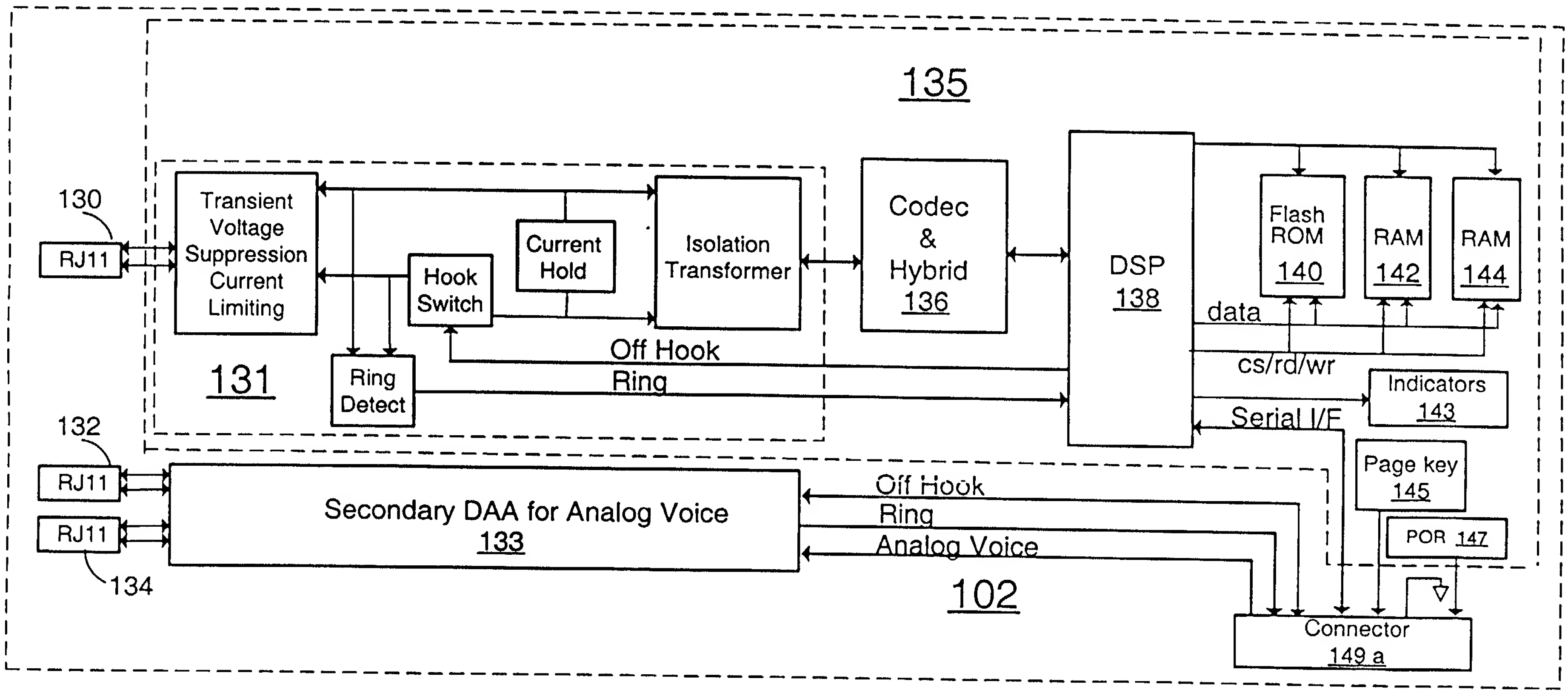

135
130
RJ11
Transient
Voltage
Suppression
Current
Limiting
Current
Hold
Hook
Switch
Isolation
Transformer
Codec
&
Hybrid
136
DSP
138
Flash
ROM
140
RAM
142
RAM
144
data
cs/rd/wr
Indicators
143
Serial I/F
Off Hook
Ring
131
Ring
Detect
132
RJ11
RJ11
134
Secondary DAA for Analog Voice
133
Off Hook
Ring
Analog Voice
Page key
145
POR 147
102
Connector
149 a

Fig. 4

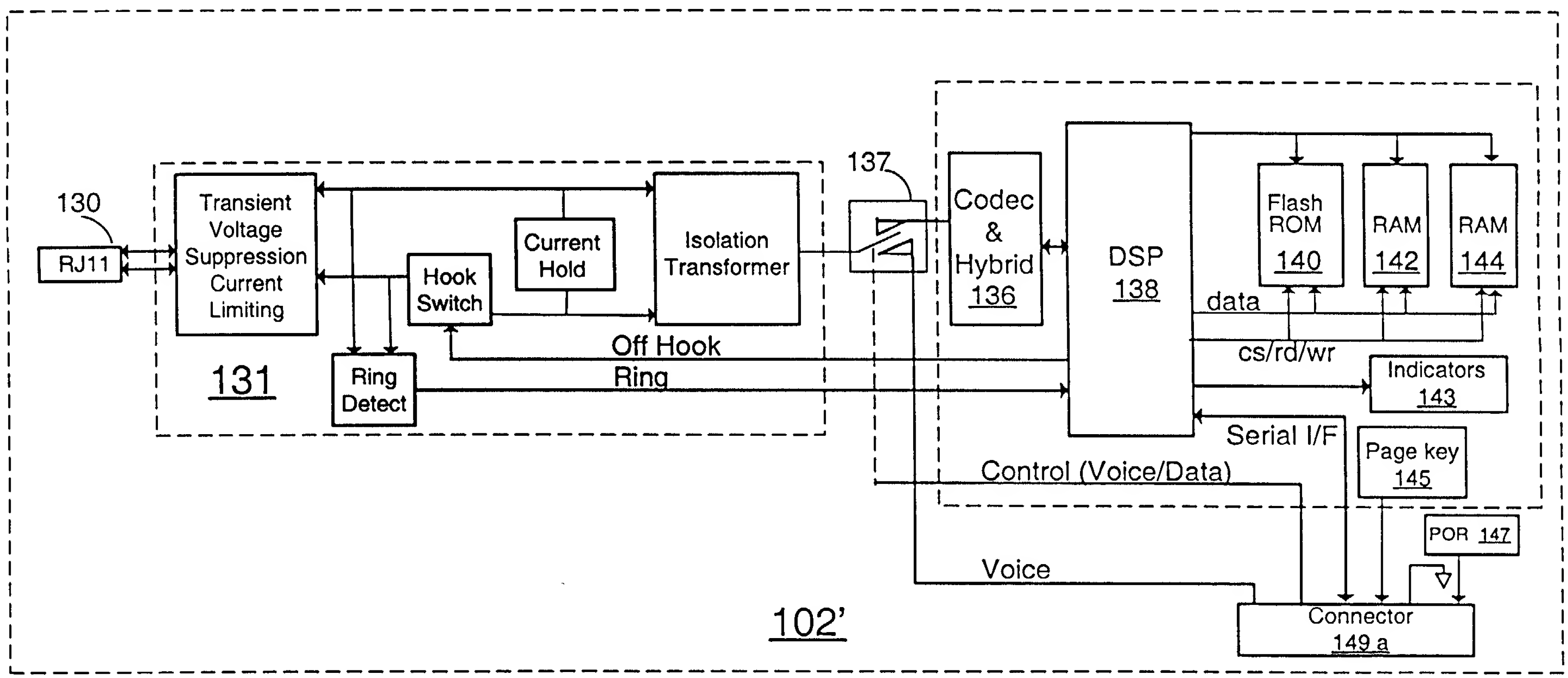
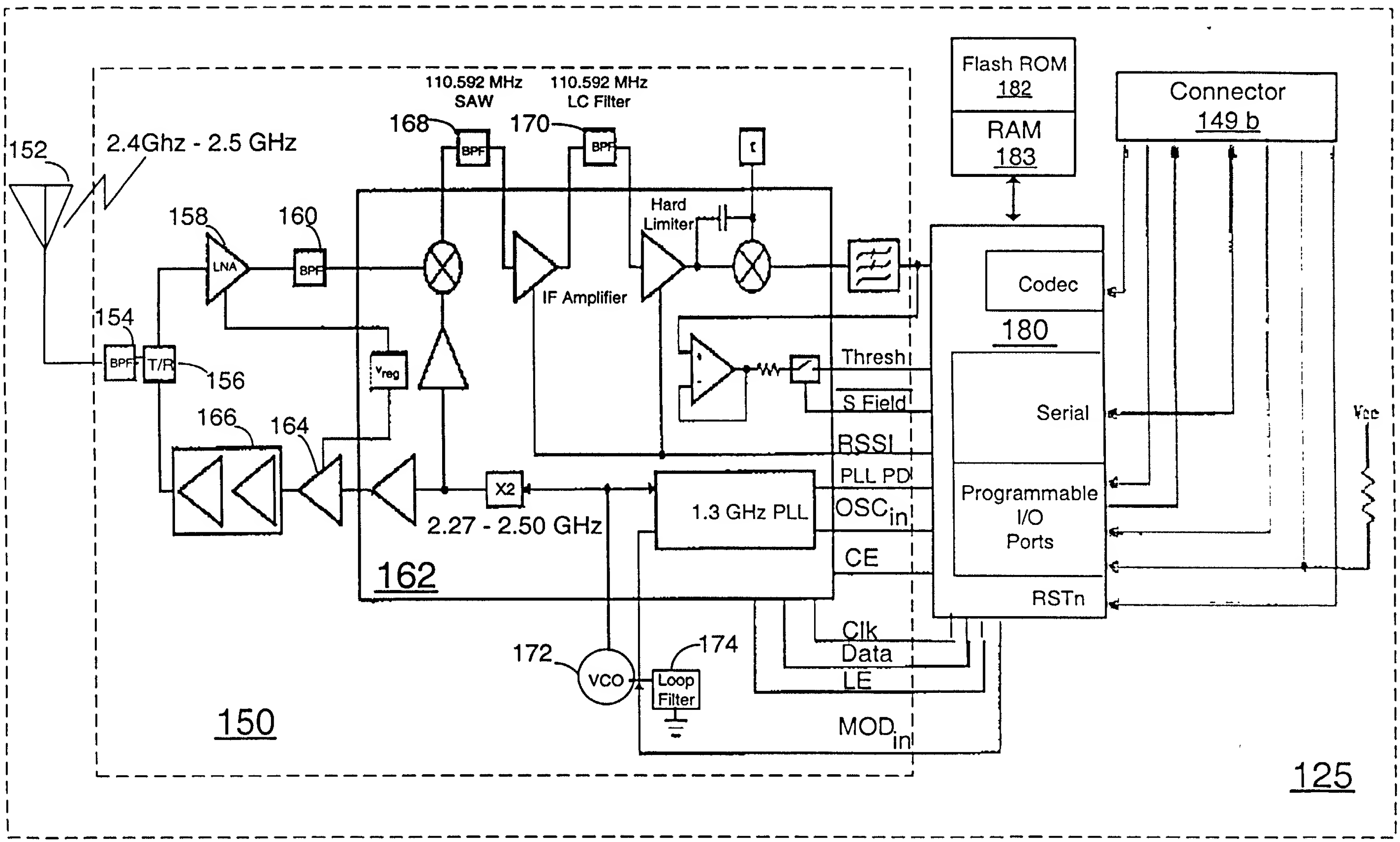

130
RJ11
Transient
Voltage
Suppression
Current
Limiting
131
Ring
Detect
Hook
Switch
Current
Hold
Isolation
Transformer
Off Hook
Ring
137
Codec
&
Hybrid
136
DSP
138
Flash
ROM
140
RAM
142
RAM
144
data
cs/rd/wr
Indicators
143
Serial I/F
Page key
145
Control (Voice/Data)
POR 147
Voice
Connector
149 a
102'

Fig. 5



152
2.4Ghz - 2.5 GHz
158
LNA
160
BPF
154
BPF
T/R
156
166
164
V_{reg}
168
110.592 MHz
SAW
BPF
170
110.592 MHz
LC Filter
BPF
IF Amplifier
Hard
Limiter
X2
2.27 - 2.50 GHz
1.3 GHz PLL
162
172
VCO
174
Loop
Filter
150
Thresh
S Field
RSSI
PLL PD
OSC_{in}
CE
Clk
Data
LE
MOD_{in}
Flash ROM
182
RAM
183
Codec
180
Serial
Programmable
I/O
Ports
RSTn
Connector
149 b
Vcc
125

Fig. 6

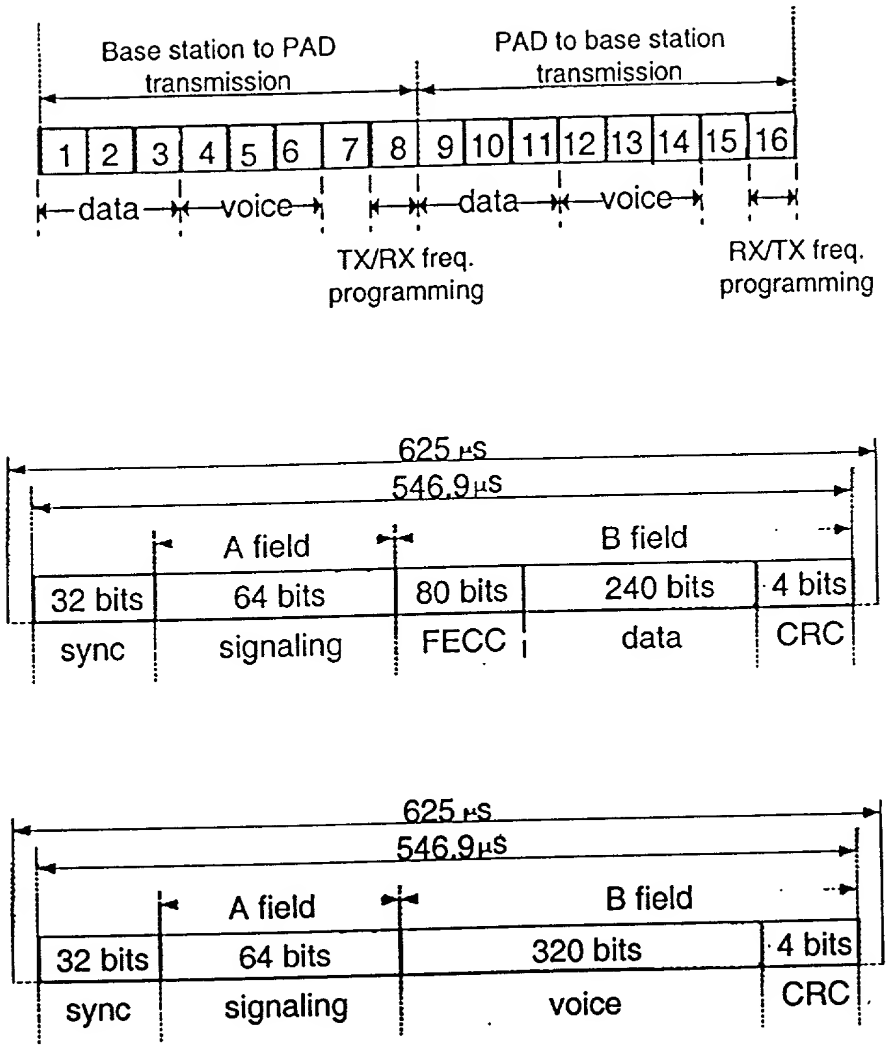


Fig. 8

PREAMBLE		HEADER			DATA
SYNC WORD 80 BITS	FRAME TIMING 16 BITS	DATA WORD LENGTH 12 BITS	DATA RATE 4 BITS	ERROR CHECK WORD 16 BITS	DATA 1-4095 BYTES

← 128 BITS →

Fig. 9
(Prior Art)

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PTO/SB/01 (12-97)
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Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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DECLARATION FOR UTILITY OR DESIGN PATENT APPLICATION (37 CFR 1.63)

[x] Declaration Submitted with Initial Filing OR [ ] Declaration Submitted after Initial Filing (surcharge (37 CFR 1.16 (e)) required)

Attorney Docket Number	P04659
First Named Inventor	Herring et al.
COMPLETE IF KNOWN	
Application Number	/
Filing Date	5 Jan. 2000
Group Art Unit	
Examiner Name	Not Assigned

As a below named inventor, I hereby declare that:

My residence, post office address, and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

DECT-Like System And Method Of Transceiving Information Over The Industrial-Scientific-Medical Spectrum

(Title of the Invention)

the specification of which

[x] is attached hereto

OR

[ ] was filed on (MM/DD/YYYY) [ ] as United States Application Number or PCT International Application Number [ ] and was amended on (MM/DD/YYYY) [ ] (if applicable).

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment specifically referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR 1.56.

I hereby claim foreign priority benefits under 35 U.S.C. 119(a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate, or 365(a) of any PCT international application which designated at least one country other than the United States of America, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or of any PCT international application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application Number(s)	Country	Foreign Filing Date (MM/DD/YYYY)	Priority Not Claimed	Certified Copy Attached? YES	NO
			[ ]	[ ]	[ ]
			[ ]	[ ]	[ ]
			[ ]	[ ]	[ ]
			[ ]	[ ]	[ ]

[ ] Additional foreign application numbers are listed on a supplemental priority data sheet PTO/SB/02B attached hereto:

I hereby claim the benefit under 35 U.S.C. 119(e) of any United States provisional application(s) listed below.

Application Number(s)	Filing Date (MM/DD/YYYY)

[ ] Additional provisional application numbers are listed on a supplemental priority data sheet PTO/SB/02B attached hereto.

Please type a plus sign (+) inside this box → [+]

DECLARATION — Utility or Design Patent Application

I hereby claim the benefit under 35 U.S.C. 120 of any United States application(s), or 365(c) of any PCT international application designating the United States of America, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of 35 U.S.C. 112, I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR 1 56 which became available between the filing date of the prior application and the national or PCT international filing date of this application.

U.S. Parent Application or PCT Parent Number	Parent Filing Date (MM/DD/YYYY)	Parent Patent Number *(if applicable)*

☐ Additional U.S. or PCT international application numbers are listed on a supplemental priority data sheet PTO/SB/02B attached hereto.

As a named inventor, I hereby appoint the following registered practitioner(s) to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith: ☐ Customer Number [ ] → *Place Customer Number Bar Code Label here*
OR
☒ Registered practitioner(s) name/registration number listed below

Name	Registration Number	Name	Registration Number
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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. 1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Name of Sole or First Inventor: ☐ A petition has been filed for this unsigned inventor

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Christopher M.	Herring

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Post Office Address	2302 Lake Park Drive						
Post Office Address							
City	Longmont	State	CO	ZIP	80503	Country	USA

☐ Additional inventors are being named on the ____supplemental Additional Inventor(s) sheet(s) PTO/SB/02A attached hereto

Please type a plus sign (+) inside this box → +

PTO/SB/02A (3-97)
Approved for use through 9/30/98. OMB 0651-0032
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DECLARATION

ADDITIONAL INVENTOR(S)
Supplemental Sheet
Page ___ of ___

Name of Additional Joint Inventor, if any: ☐ A petition has been filed for this unsigned inventor

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Inventor's Signature						Date	
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City	Lafayette	State	CO	ZIP	80026	Country	USA

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Inventor's Signature						Date	
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Name of Additional Joint Inventor, if any: ☐ A petition has been filed for this unsigned inventor

Given Name (first and middle [if any])				Family Name or Surname			
Inventor's Signature						Date	
Residence: City		State		Country		Citizenship	
Post Office Address							
Post Office Address							
City		State		ZIP		Country	

ADVANCE INFORMATION V 0.41

National Semiconductor

SC14424
Complete Baseband processor for DECT Base Stations with Caller-id and Handsfree

General Description

The SC14424 is a 3.3 Volt CMOS IC optimized to handle all the audio, signal and data processing needed within a DECT base station. An ADPCM transcoder, a very low power 14 bit Codec and Analog Frontend are integrated. Direct connections towards analog or ISDN line interface.

The SC14424 has an on-chip dedicated flexible DSP optimized for telecom applications caller-id, handsfree and allows easy connection to digital telephone answering machine devices.

The SC14424 is designed to be compatible with many radio interfaces. A dedicated TDMA controller handles all physical layer slot formats and radio control. The integrated National Semiconductor's standard CR16B processor core takes care of all the higher protocol stack. Programmable I/O ports can be configured as chip selects for I/O expanders, Serial Flashes, interrupt source or I/O. A digital serial interface can be configured to interface to industry-standard codecs and ISDN devices with μ-Law, a-Law, linear or transparent data formats. 4kByte Flash is integrated for parameter and number storage (first version not included).

Features

- Integrated DECT base band transceiver optimized for GAP base stations according to ETS 300 175-2,3 & 8.
- 2.7 to 3.3 Volt operating voltage.
- Embedded 16 bit CompactRISC™ CR16B Microprocessor with In System Emulation (ISE) mode.
- On-chip 6kByte Data Memory.
- Upto xxxkByte ROM/Flash (first version with external ROM)
- 32 kbit memory mapped Flash and BootROM (first version without Flash)
- Embedded flexible dedicated DSP executing Caller-id (CID), Caller-id on Call Waiting (CIDCW) and handsfree, two echo cancellers, two echo suppressors, extended DTMF detection, DTMF generation, sidetone and artificial echo loss.
- Two full duplex 32 kbits/sec ADPCM transcoder.
- Embedded programmable Dedicated Instruction Processor (DiP) for all TDMA based events.
- Protected and unprotected half, full and double slot B-fields D00, D08, D32 and D80
- Standard DECT encryption with different keys for different MAC-connections.
- 6 MAC connections can be handled simultaneously.
- Flexible three wire interface to radio front synthesizer.
- One 14-bit linear CODEC with programmable gain
- Peak hold ADC for RSSI measurement
- Two input 8 bit successive approximation ADC.
- Three general purpose I/O ports with programmable interrupts.
- Full duplex UART, SPI™ and MICROWIRE™ interface.
- Flexible 8 kHz synchronous Serial interface to external codecs and ISDN interface circuits.
- Two general purpose timers and watch dog timer.
- Programmable chip selects to 8 bit wide ROM, SRAM NAND Flash Memory and I/O expanders.
- Two Capture timers for frequency measurement for e.g. metering, ringing and call progress tone detection.
- 100 pin TQFP-100 package.

Note 1: CompactRISC™ is a trademark of National Semiconductor Corporation, SPI™ is a trademark of Motorola.

System Diagram

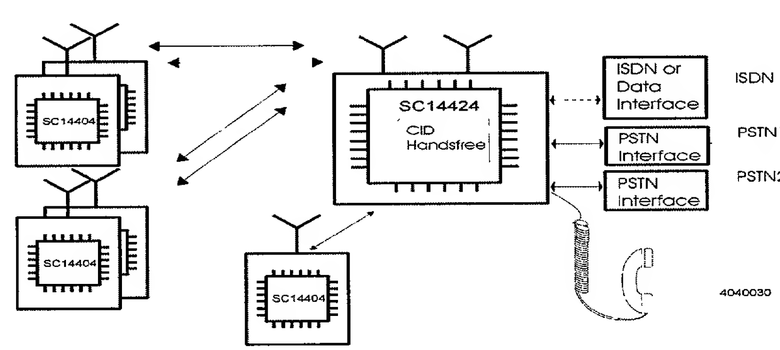
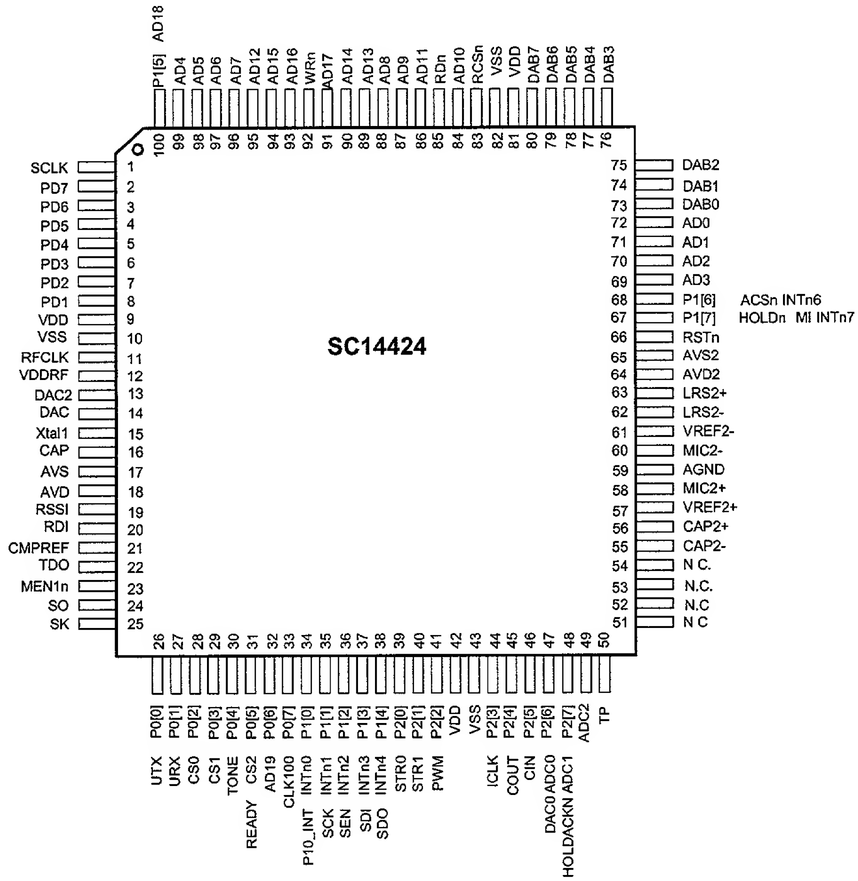


Table of Contents

1.0 Connection diagram



2.0 Pin description

Table 1: Pin Description (See chapter 5.1 for pin type definitions)

PIN NAME	NR	TYPE	DESCRIPTION
SCLK	1	1	OUTPUT/INPUT. CR16B bus interface System CLocK output.
$PD_{7..1}$	2-8	5	TRISTATE OUTPUT. Programmable Power Down pins 7 to 1 to radio interface. PD7,6,5 have 12 mA drive. PD0 internally controls the peak hold circuitry (See pin RSSI).
VDD	9		Digital supply voltage
VSS	10		Digital ground
RFCLK	11	5b	OUTPUT (Slope controlled). 10.368 MHz clock output. Logic '0' after reset or when disabled.
VDDRF	12		Supply voltage for RFCLK, XTAL DAC, DAC2 output pads.
DAC2	13	analog	OUTPUT. 8 bit DAC output 2.
DAC	14	analog	OUTPUT. 8 bit DAC output E.g. for frequency control.
Xtal1	15	analog	INPUT. 10.368 MHz crystal connection.
CAP	16	analog	External capacitor for crystal oscillator.
AVS	17		Analog ground.
AVD	18		Analog supply.
RSSI	19	analog	INPUT. Receiver Signal Strength Indication. This signal is connected to a 6-bit ADC input with peak hold circuitry. PD0 internally controls the peak hold circuitry. If PD0 is low RSSI is sampled, else the RSSI input will be connected to ground.
RDI	20	analog	INPUT. Received Data. The polarity of this input is programmable.
CMPREF	21	analog	INPUT. Comparator reference level. Internally a six bit DAC can be connected to this pin to compensate for DC offsets.
TDO	22	5/analog	TRISTATE OUTPUT. Transmit Data. The polarity of this output is programmable.
MEN1n	23	5	OUTPUT. Programmable Load Enable for synthesizer.
SO	24	1	TRISTATE OUTPUT. Serial data output.
SK	25	5	OUTPUT. Serial interface clock: 1.152 MHz
P0[0] or UTX	26	2	INPUT/OUTPUT with selectable pull up resistor. General purpose memory mapped I/O port bit. UART data output.
P0[1] or URX	27	3	INPUT/OUTPUT with selectable pull down resistor. General purpose memory mapped I/O port bit. UART data input.
P0[2] or CS0	28	2	INPUT/OUTPUT with selectable pull up resistor. General purpose memory mapped I/O port bit. Multi function Chip select output CS0
P0[3] or CS1	29	2	INPUT/OUTPUT with selectable pull up resistor. General purpose memory mapped I/O port bit. Multi function Chip select output CS1
P0[4] or TONE	30	2	INPUT/OUTPUT with selectable pull up resistor. General purpose memory mapped I/O port bit. TONE input to capture timer. (E.g. metering tones)
P0[5] or CS2 or READY	31	3	INPUT/OUTPUT with selectable pull down resistor. General purpose memory mapped I/O port bit. Multi function Chip select output CS2 If P0[5] is configured as READY pin then if HOLDn is '1', this pin will become low upon a read or write access by an external processor.
P0[6] or AD19	32	3	INPUT/OUTPUT with selectable pull down resistor. General purpose memory mapped I/O port bit. OUTPUT Address bit 19.
P0[7] or CLK100	33	2	INPUT/OUTPUT with selectable pull up resistor. General purpose memory mapped I/O port bit. OUTPUT 100 Hz clock synchronized to 10 msec frame.
P1[0] or P10_INT	34	2	INPUT/OUTPUT with selectable pull up resistor and 12 mA sink capability. General purpose memory mapped I/O port bit. Level sensitive interrupt source P10_INT
P1[1] or SCK	35	2	INPUT/OUTPUT with selectable pull up resistor and 12 mA sink capability. General purpose memory mapped I/O port bit. SPI Clock input/output

Table 1: Pin Description (See chapter 5.1 for pin type definitions)

PIN NAME	NR	TYPE	DESCRIPTION
P1[2] or SEN	36	2	INPUT/OUTPUT with selectable pull up resistor and 12 mA sink capability. General purpose memory mapped I/O port bit. SPI Clock enable input if SPI slave. If SPI master this pin must be set/reset by software.
P1[3] or SDI	37	2	INPUT/OUTPUT with selectable pull up resistor and 12 mA sink capability. General purpose memory mapped I/O port bit. SPI data input
P1[4] or SDO	38	2	INPUT/OUTPUT with selectable pull up resistor and 12 mA sink capability. General purpose memory mapped I/O port bit. SPI data output
P2[0] or STR0	39	1	INPUT/OUTPUT. General purpose memory mapped I/O port bit. OUTPUT External codec interface STR0 .
P2[1] or STR1	40	1	INPUT/OUTPUT. General purpose memory mapped I/O port bit. INPUT/OUTPUT. External codec interface strobe STR1.
P2[2] or PWM	41	4	INPUT/OUTPUT. General purpose memory mapped I/O port bit. OUTPUT. Pulse width Modulation with open drain with 100mA sink capability. The pulse width and frequency is controlled with TIMER0.
VDD	42		Digital supply voltage.
VSS	43		Digital ground.
P2[3] or ICLK	44	1	INPUT/OUTPUT. General purpose memory mapped I/O port bit. INPUT/OUTPUT. External codec interface clock. On falling edge data is valid.
P2[4] or COUT	45	4	INPUT/OUTPUT. General purpose memory mapped I/O port with open drain. INPUT/OUTPUT. External interface data input, codec output with open drain.
P2[5] or CIN	46	1	INPUT/OUTPUT. General purpose memory mapped I/O port bit. INPUT/OUTPUT. PCM interface data output, codec input.
P2[6] or ADC0 or DAC0	47	5/analog	DIGITAL OUTPUT/ANALOG INPUT. General purpose digital output. General purpose input to 8 bit ADC. 8 bit DAC if neither ADC0,1 nor 2 are selected.
P2[7] or ADC1 or HOLDACKn	48	5/analog	DIGITAL OUTPUT/ANALOG INPUT. General purpose digital output. General purpose input two to 8 bit ADC. This pin can be configured as active low HOLD acknowledge output.
ADC2	49	analog	ANALOG INPUT. General purpose input three to 8 bit ADC.
TP	50	1	INPUT. Test input. Must be 0 for normal operation.
N.C.	51		Not connected
N.C.	52		Not connected
N.C.	53		Not connected
N.C.	54		Not connected
CAP2-	55	analog	External capacitor 1 for codec 2 DC offset blocking.
CAP2+	56	analog	External capacitor 2 for codec 2 DC offset blocking.
Vref2+	57	analog	OUTPUT. Positive microphone 2 reference voltage.
MIC2+	58	analog	INPUT. Microphone positive 2 input.
AGND	59	analog	Signal ground.
MIC2-	60	analog	INPUT. Microphone 2 negative input.
Vref2-	61	analog	OUTPUT. Negative microphone 2 reference voltage.
LRS2-	62	analog	OUTPUT. Negative loudspeaker 2 output.
LRS2+	63	analog	OUTPUT. Positive loudspeaker 2 output.
AVD2	64		Analog supply.
AVS2	65		Analog ground.
RSTn	66	4	INPUT/OUTPUT. Active low Reset with open drain output. Will be pulled low if the supply voltage goes below 2.7V.

Table 1: Pin Description (See chapter 5.1 for pin type definitions)

PIN NAME	NR	TYPE	DESCRIPTION
P1[7] or HOLDN or MI	67	2	INPUT/OUTPUT. General purpose memory mapped I/O port bit with selectable pull-up resistor. If used as input the start-up level must be '1'. INPUT. P1_MODE_REG can select this pin as HOLDn input. If HOLDn is set to '0', the CR16B processor will terminate its current instruction and the ADx, WRN, RDN will go tristate. In this mode an external CR16B can control the SC14424 completely. In emulation mode this pin is selected as MI output. MI goes high if an internal interrupt is asserted.
P1[6] or ACSn	68	2	INPUT/OUTPUT. General purpose memory mapped I/O port bit with selectable pull-up resistor. OUTPUT. Auxiliary Chip Select not. This signal becomes low if the address range is within the programmed address range.
AD3..0	69-72	1	OUTPUT. Address bit 3 to 0. In HOLD mode these pins are input.
DAB0..7	73-80	1	INPUT/OUTPUT. Data bus bit 0..7.
VDD	81		Digital supply voltage.
VSS	82		Digital ground.
RCSn	83	5	OUTPUT. ROM Chip Select not. Low active if none of the internal peripherals or the ACSn is addressed.
AD10	84	1	OUTPUT. Address bit 10. In HOLD mode this pin is input.
RDn	85	1	OUTPUT. Active low read. In HOLD mode this pin is input.
AD11	86	1	OUTPUT. Address bit 11. In HOLD mode this pin is input.
AD9	87	1	OUTPUT. Address bit 9. In HOLD mode this pin is input.
AD8	88	1	OUTPUT. Address bit 8. In HOLD mode this pin is input.
AD13	89	1	OUTPUT. Address bit 13. In HOLD mode this pin is input.
AD14	90	1	OUTPUT. Address bit 14. In HOLD mode this pin is input.
AD17	91	1	OUTPUT. Address bit 17. In HOLD mode this pin is input.
WRn	92	1	OUTPUT. Active low write signal. In HOLD mode this pin is input.
AD16,15, 12	93-95	1	OUTPUT. Address bit 16,15 & 12. In HOLD mode these pins are input.
AD7-4	96-99	1	OUTPUT. Address bit 7 to 4. In HOLD mode these pins are input.
P1[5] or AD18	100	2	INPUT/OUTPUT. General purpose memory mapped I/O port bit with selectable pull-up resistor. OUTPUT Address bit 18.

NOTE: All digital outputs can sink/source 2 mA unless otherwise specified. All digital inputs are Schmitt trigger types. After reset all I/Os are set to input and all pull-up or pull-down resistors are enabled. The p0[0] pull-up resistor is disabled at start-up.
All digital inputs can handle upto 5V input levels, provided that the SC14424 VDD is supplied with its operating voltage.

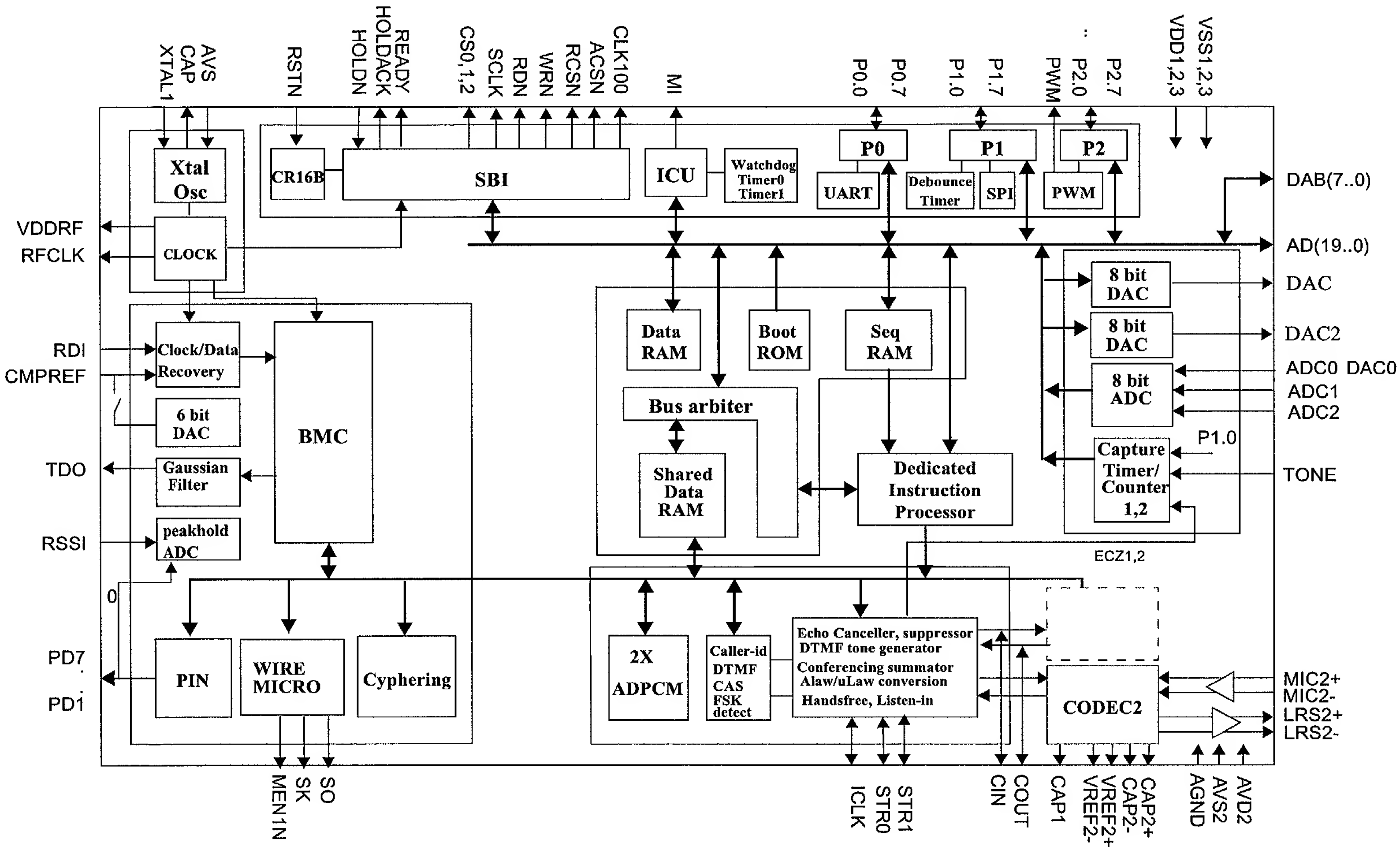


FIGURE 1. SC14424 Block diagram

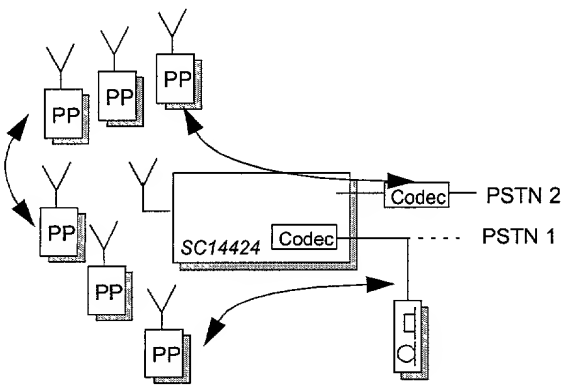
3.0 General description

3.1 SYSTEM FUNCTIONS

The SC14424 is a very highly integrated IC Baseband processor for DECT base stations. It can be used in residential, small office small home application as well as wireless local loop. In addition to the DECT Burst mode controller and two G.721 ADPCM transcoders, it provides functions for Half duplex speakerphone, Listening-in, Caller-id, Caller-id on call waiting and supports high speed modem transfer for Cordless terminal adapters.

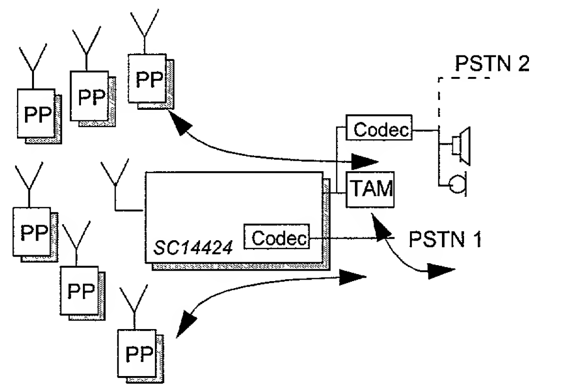
One or more handsets or portable parts (PP), can communicate via one radio receiver or fixed part (FP), with each other or to the outside world, either via a PBX or not. The SC14424 is optimized for use in a domestic base station connected via an analog line interface to the central office. A second echo canceller and suppressor allows for two line application, a handsfree speakerphone, listening-in or a corded phone connection. A digital interface to an external codec allows for a two line application.

Figure 1 gives an functional overview of the domestic applications.

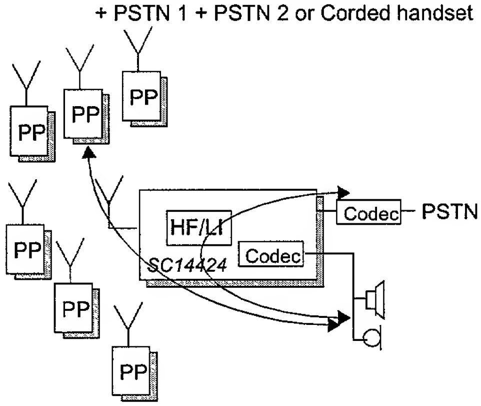


Conversations
* Cordless handset 1 to PSTN 1
* Cordless handset 2 to PSTN 2
  or Corded Handset to PSTN 2
* Handset to Handset

4 party conferencing
Cordless handset 1 + Cordless handset 2
+ PSTN 1 + PSTN 2 or Corded handset

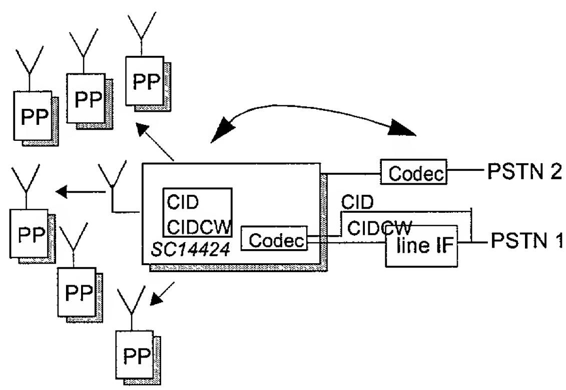


External Telephone answering Machine (TAM)
During conversation Cordless handset to PSTN
Recording and playback through
* Second Cordless Handset
* or External PSTN line 2
* or Base station loudspeaker
Remote DTMF control



Handsfree Speakerphone (HF)
* During conversation Cordless handset to PSTN1
  Handsfree to Cordless handset

Listening-in (LI)
* During TAM recording/playback
* Multi party conversation PP1, PP2, PSTN1



Caller-id (On-hook CID)
Caller-id on Call Waiting (off-hook CIDCW)
1 line support for on-hook CID
Line 1 or line 2 CIDCW

Bell 202, V23, DTMF standards

FIGURE 1. Domestic applications

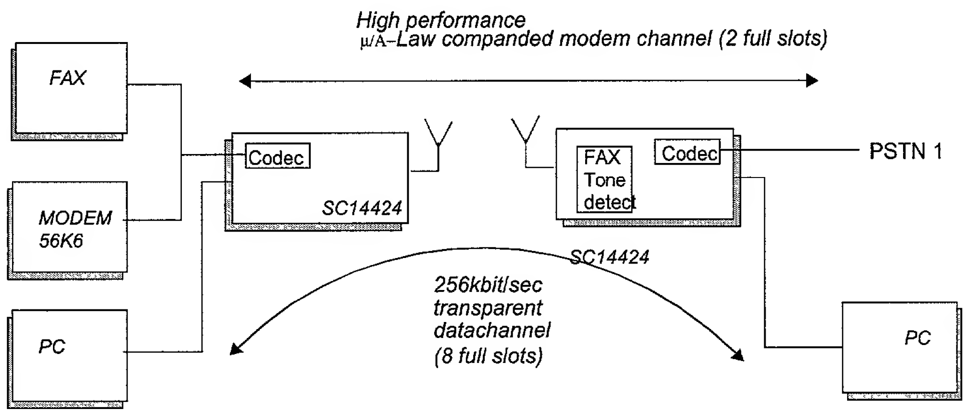


FIGURE 2. Data application for CTA and WLL

The SC14424 is equipped with a flexible dedicated Digital Signal Processing unit which handles tone generation, conferencing and echo cancelling and suppression. In case of ISDN for both B channels echo suppression can be selected. The DSP also performs Caller-id and DTMF detection.

More SC14424's can be connected in parallel to allow for a modular approach with more external lines.

The SC14424 used in a base station can handle 6 MAC connections. A typical configuration has two handsets communicating to two external lines while the other MAC connections can be used for internal calls.

For every MAC connection a different encryption key can be used simultaneously.

4.0 Functional description

4.1 EMBEDDED MICROCONTROLLER

4.1.1 CR16B CompactRISC™ and peripherals

The SC14424 has an on-chip 16 bits CR16B Compact RISC™ microprocessor. It executes from on-chip boot ROM, from on-chip RAM or from external memory. The CR16B accesses on-chip peripherals like Dedicated Instruction Processor (DIP), Sequencer RAM, Ports P0, P1, P2. A multi level multi source Interrupts Control Unit (ICU) determines interrupt priorities and generates exception vectors.

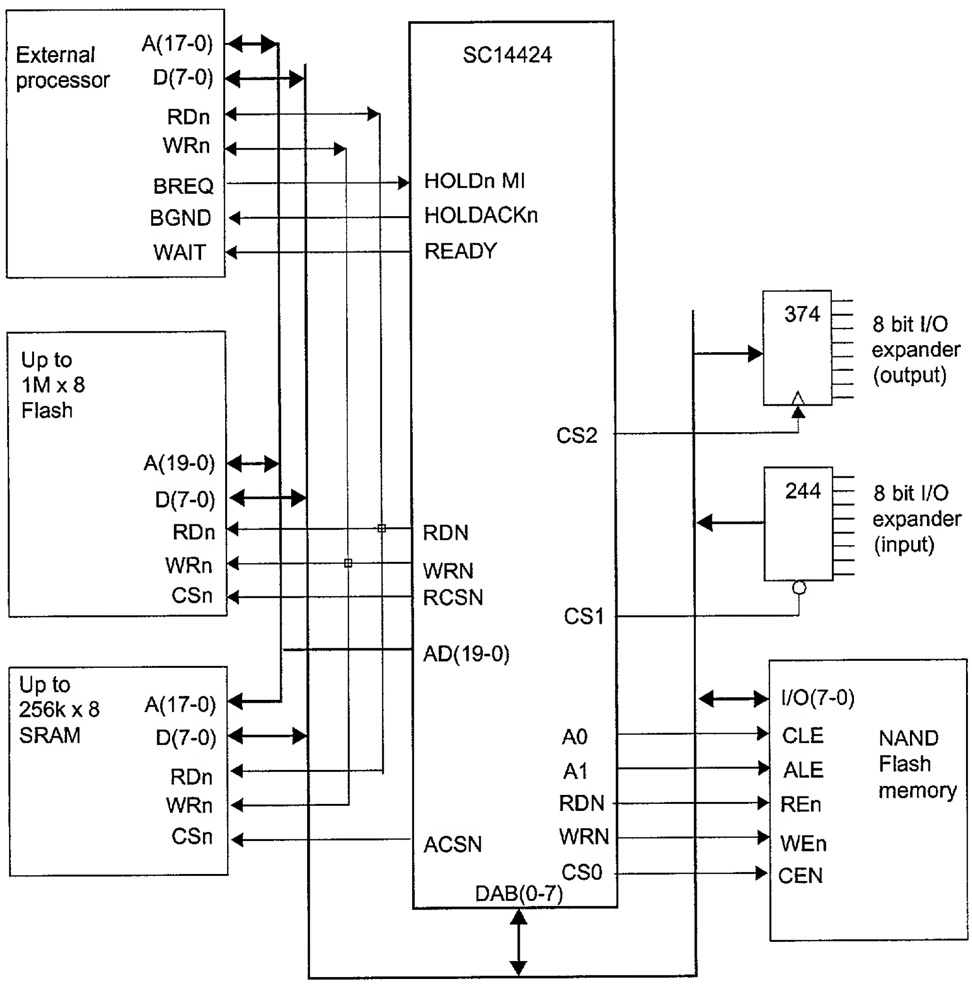


FIGURE 3. System Bus interface

4.1.2 System Bus interface (SBI)

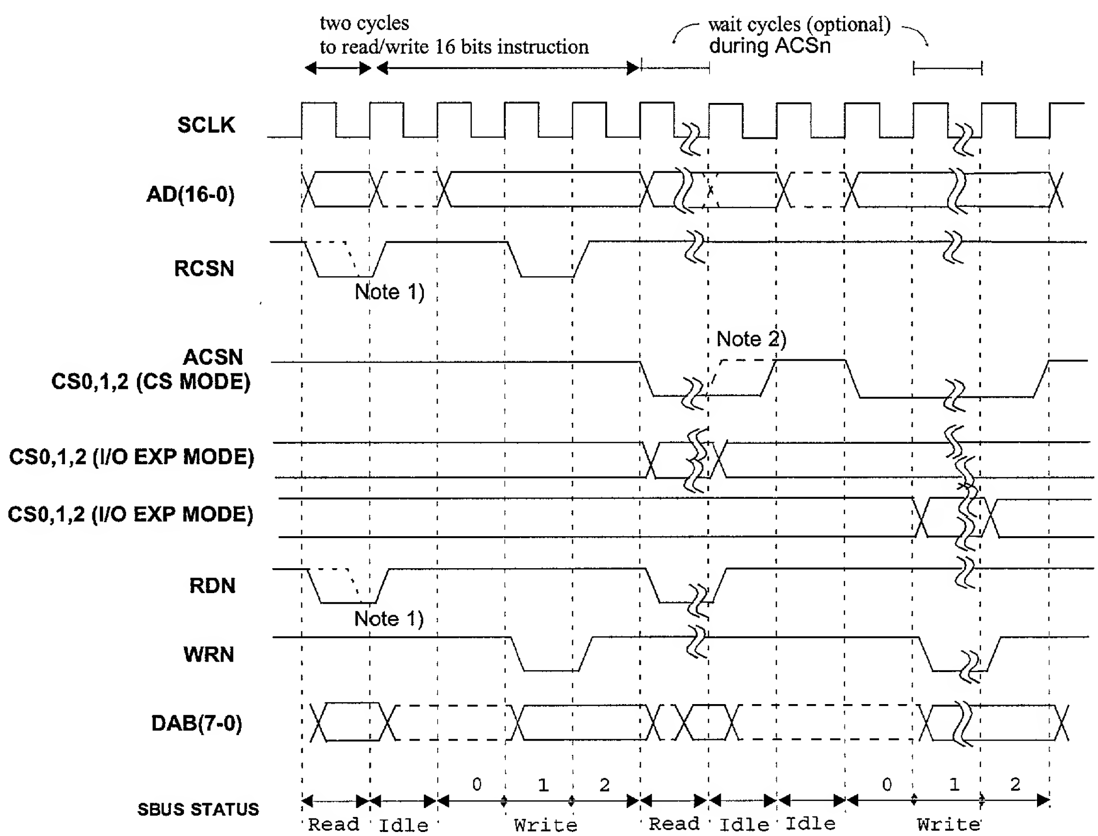
The SC14424 supports access to external 8 bits wide ROM, Flash, SRAM or memory mapped I/O and allows Direct Memory Access (DMA) by an external processor to all on and off chip peripherals.

The CR16B core interfaces via the System Bus Interface (SBI) unit to all on-chip and off-chip peripherals. The SBI generates the read and write control signals, chip selects and converts 8-bit system bus to the 16-bits CR16B core bus.

The SBI interface signals are:

- AD0-AD19. Address signals allowing an addressable range upto 1Mbyte. In HOLD mode, AD0 to AD19 are input and decoded for RCSN, ACSN, CSx.

- DAB0-DAB7. Bidirectional Data bus 0-7.
- RDN, WRN Read/write active low outputs for all memories.
- RCSN. ROM chip select. Active low output. See memory map for selected range.
- ACSN. Auxiliary chip select for SRAM or memory mapped I/O. Active low output. The active range as well number of wait cycles is programmable for this chip select. See memory map for selected range.
- HOLDn/MI. Active low input/output. Selects CR16B hold mode if '0'. In HOLD mode the internal CR16B terminates its last instruction cycle and sets ADx, RDN, WRN as input and will be synchronised with SCLK. An external processor has now full access over the internal and external memory locations. Internal pull-ups resistors prevent floating pins. In emulation mode this pin becomes Maskable Interrupt output MI.
- HOLDACKN. Active low output. If low the SC14424 has terminated its current instruction and the external address and data bus are released.
- READY. Active HIGH output. In HOLD mode, READY will be LOW when reading or writing to the shared DataRAM as long as the internal peripheral have access to the DataRAM. The low period depends on the system clock division ratio (see 4.2). (3 SCLK cycles, writing to shared RAM in case of div1, 4 SCLK cycles, reading from shared RAM in case of div1, 2 SCLK cycles, reading from shared RAM in case of div2/div3, 0 SCLK cycles in case of > 3).
If other memory locations are accessed READY is LOW during one SCLK synchronisation cycle.
- SCLK, Buffered System clock output.
- CS0, CS1, CS2. Chip selects outputs with programmable function. If configured for I/O expansion, the outputs become active low or active high during a read or write operation to a selective address range (CS0:$FF70_{16}$ to $FF7F_{16}$, CS1:$FF80_{16}$ to $FF8F_{16}$, CS2:$FF90_{16}$ to $FF9F_{16}$. If configured as chip selects then the outputs become active if as soon as the address is in the selected range. (See Figure 4). In this mode the selected device still needs RDN or WRN signal to read from or write to.



Note 1: RCSn, RDn are 3 SCLK cycle low for Clock divider N > 3 and ROM is read, else N SCLK cycles
Note 2: ACSn is extended with one SCLK cycle if the CR16 reads a byte in stead of a word and the number of waitcycles is even.

FIGURE 4. SBI timing

4.1.3 Normal mode

If pin TP is LOW and an pin RSTn gets a low pulse, the SC14424 resets and starts its normal operation. (See also boot ROM selection)

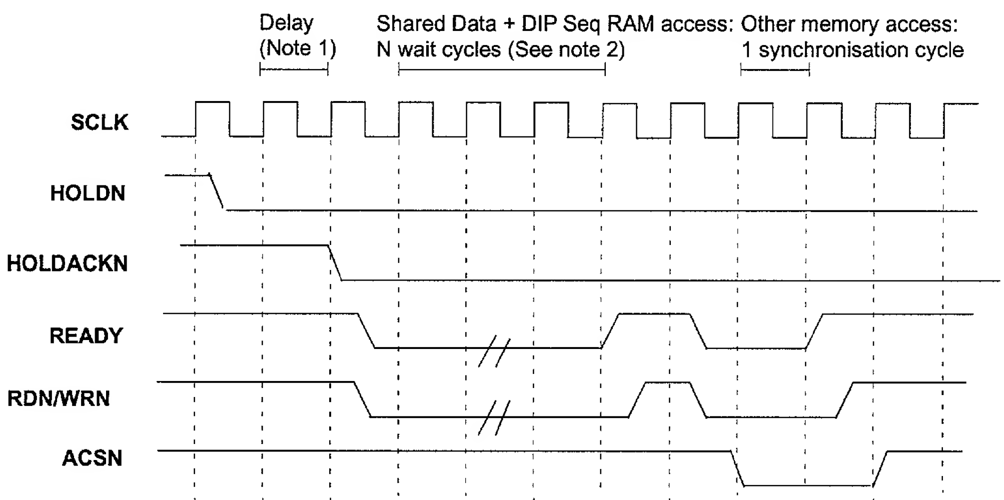
4.1.4 HOLD mode

The SC14424 internal CR16B processor can be stopped to allow an external processor to access all on-chip and off-chip memories and registers. If the HOLDn pin is set LOW, the internal CR16B terminates its internal instruction and switches AD0-AD19, RDN, WRN as input.

If an external processor accesses the shared internal Data RAM, the access cycle times must be stretched to allow undisturbed access (See figure 5)

4.1.5 Emulation mode

The emulation mode is equal to HOLD mode except that the HOLDn input becomes Maskable Interrupt output which generates an interrupt if an internal interrupt is asserted. Emulation mode is enabled when HOLDn is LOW during the rising edge of RSTN. The READY pin is automatically set to output if emulation mode is selected. In emulation mode the CR16B will be kept in reset state. To leave the emulation mode, the HOLDn pin must be HIGH on the rising edge of RSTn.



Note1: Delay: X cycles

Note2: CLK_DIV_REG = 1,2 or 3 then number of wait cycles is 4,2,2
else number of wait cycles is 1.

FIGURE 5. External processor timing in HOLD mode

4.1.6 System reset

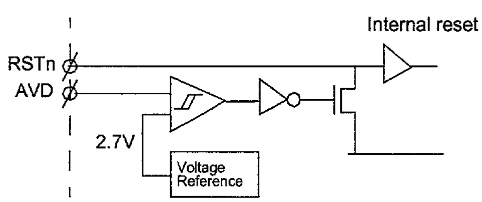


FIGURE 6. System reset

The SC14424 will be reset if either RSTn is pulled low externally or if the voltage on AVD goes below 2.7 VDD. In this way an wired "OR" function with an external RC circuitry can be made.

4.2 MEMORIES

4.2.1 Boot ROM

The SC14424 has a small boot ROM. The boot ROM is located at 0 to $3FF_{16}$. After a hard reset the on-chip boot code is executed if the UART-Rx pin Po[1] is pulled high by an external device such as a PC upon a hard reset. If nothing is connected to Po[1], it is pulled down, with an internal pull-down resistor from reset, and the normal program will be executed. Depending on the status of the environment register bits (P0_ENV_REG[2]) the on-chip boot program starts executing from address 0 or 10000_{16}. The P0_ENV_REG is loaded from Port 0 at reset.

If DEBUG_REG[5] is set to '1' the internal boot rom can be disabled on a software reset. The boot ROM loads an application program into the internal DataRAM received on the UART-Rx pin. Once a complete program is loaded

into RAM the CR16 starts executing from RAM location $D800_{16}$. This allows to program external flash devices using a defined program.

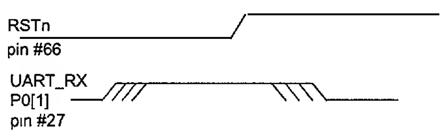


FIGURE 7. Boot rom selection

4.2.2 Internal Data RAM

The 8,5 kByte of internal memory is divided over five sections:

- A block of 4,5kByte which can only be accessed by the CR16B. This memory is used to store CR16B program and variables.
- A block of 2kByte which can be accessed by CR16B, ADPCM, BMC, DIP, MICROWIRE, Cyphering and PIN. This memory is used to allocate DECT control, transmit and receive data.
- A block of 1kbyte which can be accessed by CR16B and the ECP to store ECP parameters.

4.2.3 DIP Sequencer RAM

The 510 bytes of internal DIP program RAM contain the DIP executable code. The executable code inside this RAM can be read and written by the CR16B at any time. An internal bus arbiter takes care of bus conflicts if the DIP and CR16B access the Data RAM at the same time. ($FA02_{16}$ to $FBFF_{16}$).

4.2.4 External ROM/RAM

The CR16B has a 21 bits addresses bus (AD0 to AD20) of which 20 bits are used for a linear address space of 1Mbyte of program memory upto 256 kbytes of data (See table 1). Address AD20 is not used in the address decoder. Pin ACSn goes always low if the address is within a programmed address range determined by AUX_CS_LOW_REG and AUX_CS_HIGH_REG. The block size determined by these registers is N*4kByte. The address range from D800-FFFF (5.5k) is used for on-chip addresses. If neither ACSn nor on-chip peripherals or memory is accessed, RCSn goes low. To save power, AD[19..0], DAB[7..0], RDn and WRn can be made inactive at internal accesses if bit EN_BUS in the DEBUG_REG is cleared. The CR16B can also write to program memory whilst executing a small program in on-chip RAM.

4.2.5 Memories for voice storage

For storage of (compressed) speech samples, the SPI can be used to store data in serial memories (Toshiba, ATMEL Dataflash^{TM}). Samsung parallel access NAND flashes can directly be connected to the data/address bus using CS0,1,2 as chip select. The chip select addresses are mapped on the on-chip peripheral register. (See chapter 4.1.2)

Table 1: Memory Map overview (grey area indicates internal area)

Address	Description
0000_{16}	Internal Boot ROM (1024 bytes)
0400_{16}	External ROM (53.5k bytes)
	External RAM
$D800_{16}$	Non shared CR16B RAM (4k bytes)
$E800_{16}$	-
$EA00_{16}$	Shared Data RAM/CR16B RAM (2k bytes)
$F200_{16}$	Shared ECP/CR16B RAM (1k bytes)
$F600_{16}$	-
$FA00_{16}$	DIP Sequencer RAM (510 + 2 bytes)
$FC00_{16}$	CR16B internal interrupt vectors
$FF02_{16}$	On-chip Peripheral Registers (see page 44)
10000_{16}	External ROM 64k-128k Small and large models 64k-1M. Large model
$FFFFF_{16}$	External RAM (64k -256k Small and large models)

4.2.6 Interrupt Control Unit (ICU)

The SC14424 has 1 non-maskable interrupt, 10 maskable interrupts and 6 exception vectors. If an interrupt source becomes active the ICU generates an interrupt. In case of a maskable interrupt source the ICU determines whether this interrupt source has the highest priority before the CR16B is forced to terminate the current instruction. In case of a non-maskable interrupt source the CR16B is always forced to terminate the current instruction. After saving the stack pointer and processor status register, the CR16B executes interrupt service procedure at INTBASE + [interrupt vector * 2]. (Small model) or INTBASE + [vector offset * 4] (Large model). The INTBASE can be stored with CR16B instruction <LPR> and must have a value divided by two. The vector addresses are shown in Table 2.

Interrupt priorities

The CR16B has four fixed interrupt priorities as shown in Table 2. The DBG interrupt has he highest interrupt, next the NMI has the highest. The ISE and exception vectors have the lowest priorities 4 and 5. The non maskable interrupts with priority 3 have a programmable sub priority level which can be set in registers xxx_INT_REG (see Table 24).

Writing priority value '000' will disable these interrupts. If more than one interrupt request occurs the one with the highest priority is accepted, the others stay pending. At the end of an interrupt service routine, the pending interrupt must be cleared by software by writing a '1' in register RESET_xxx_INT_PENDING_REG (see Table 20). This register also gives the status of the pending interrupt if read.

If maskable interrupts have the same interrupt levels the inherent priority scheme is used. The DIP interrupt has the highest inherent priority. The watchdog timer will generate an NMI.

Table 2: SC14424 Interrupt Vectors

Interrupt source	Vector Address (Small model)	CR16B Interrupt priority	Mask. int Inherent sub priority
NMI	INTBASE + 02_{16}	2	-
reserved	INTBASE + 04_{16},06_{16},08_{16}	-	-
SVC	INTBASE + $0A_{16}$	5 (exceptions)	-
DVZ	INTBASE + $0C_{16}$		
FLG	INTBASE + $0E_{16}$		
BPT	INTBASE + 10_{16}		
TRC	INTBASE + 12_{16}		
UND	INTBASE + 14_{16}		
Reserved	INTBASE + 16_{16},18_{16},$1A_{16}$	-	
DBG	INTBASE + $1C_{16}$	1	-
ISE	INTBASE + $1E_{16}$	4	-
TONE	INTBASE + 20_{16}	3	lowest
CLK8K	INTBASE + 22_{16}	3	
KEYBRD	INTBASE + 24_{16}	3	
P10_INT	INTBASE + 26_{16}	3	
UART	INTBASE + 28_{16}	3	
SPI	INTBASE + $2A_{16}$	3	
TIM0	INTBASE + $2C_{16}$	3	
TIM1	INTBASE + $2E_{16}$	3	
CLK100	INTBASE + 30_{16}	3	
DIP	INTBASE + 32_{16}	3	highest

4.3 SYSTEM CLOCK GENERATION

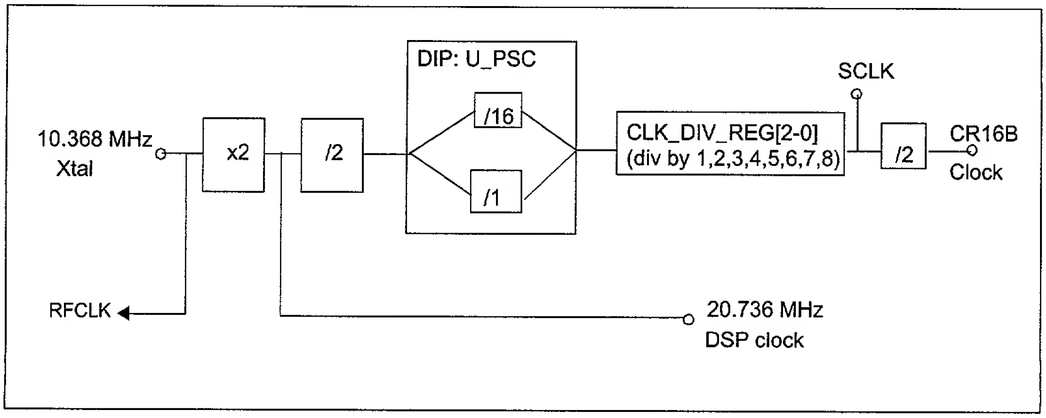
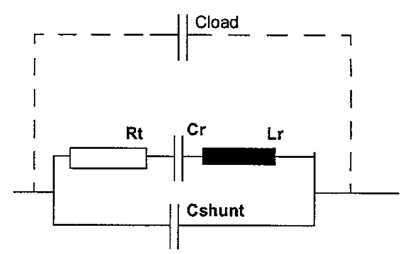


FIGURE 8. System clock selection

The SC14424 contains an amplitude controlled oscillator which can run at 10.368 MHz. This oscillator is designed for power saving.

The Xtal frequency can tuned using a varicap and one of the on-chip DACs. (See page 38).

The SBI generates the internal timing signal and clock signals for the system bus. For power saving in PP mode, the CR16B clock can be divided from the crystal clock frequency by means of CLK_DIV_REG (values: 1,2,3,4,5,6,7,8). With DIP Sequencer command <U_PSC> an extra divide factor 16 can be selected with the prescaler. Modifying the CLK_DIV_REG or generating an DIP interrupt when the prescaler is enabled, results in an immediate clock frequency change.

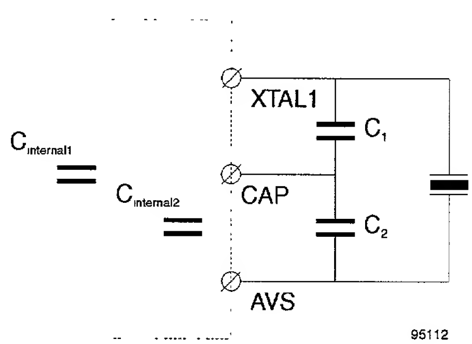


Xtal equivalent circuit + Cload

FIGURE 10. Crystal specification

Table 3: Crystal specification

PARAMETERS	MAXIMUM VALUE
C Load	41 pF
Rt	75 Ω
CShunt	7 pF



$$\text{Cload} = \frac{\text{C1 x (C2 + Cinternal2)}}{\text{C1 + (C2 + Cinternal2)}} + \text{Cinternal}$$

Cinternal < 3 pF

FIGURE 9. Crystal connection

4.4 DEDICATED INSTRUCTION PROCESSOR (DIP)

The SC14424 contains a Dedicated Instruction Processor (DIP). The instructions for the DIP are stored in the Sequencer Random Access Memory. The DIP takes care of all the slot and frame timing to the RF front end interface without microprocessor interruption. All necessary data and control information can be stored in advance to control a complete 10ms frame without microprocessor interruptions even if more slots with different data areas are used. Consecutive instructions are performed at the symbol clock rate. Eight programmable timing signals (PD(7:0)) are provided to control, activate or deactivate the RF front end. These timing signals can be set or reset by instructions which are loaded into the sequencer memory. This permits flexible connection to different RF frontends. Every symbol period a new instruction is fetched thus these signals can be set/reset with a resolution of 1 symbol period. As an example figure 12 shows the timing of the ARi1 interface.

The sequencer RAM program allows for jumps to subroutines upto 4 deep and unconditional branches. A WNT {wait N symbols} opcode puts the sequencer RAM in a mode where it waits N symbol periods before the next instruction is performed. The WT {Wait for next slot} opcode waits to process the next instruction until the active slot is finished.

If enabled (e.g. in the PP mode) the next slot counter is synchronized to the received frame structure. In paging mode, both normal and slow scan, the programming is such that only once every 16 or 64 frames the sequencer RAM program is looped.

Specific instructions in the sequencer memory control the location of the data storage in the data RAM.

With this implementation one has the possibility, with a resolution equal to the symbol clock (870ns) to:

1) Set or reset at any moment the PD(7:0) signals.
2) Receive and or transmit in any (or all) timeslot(s).
3) Preprogram different A-field data messages
4) Program different synthesizer programs for any slot without μC interruption
5) Program normal and low speed paging
6) Program interrupts at any time in the frame
7) Program receive levels
8) Control the ADPCM mute, sidetone and receive levels.
9) Program test loops
10) Program Power Down modes.
11) Handle encryption on all slots
12) Program protected B-field formats
13) Format half, full and double slots
14) To build any other user defined format.

4.4.1 DIP interfacing to CR16

The SC14424 CR16B controls the DIP with the DIP control register. Information between the CR16B and the DIP are exchanged through dual ported memory (Sequencer RAM, Shared Data RAM). At initialization the CR16B has to take care that the sequencer program is stored in this sequencer RAM. With bit 7 set to '1' in the control register, the chip will reset to its initial state. Data is retained in the memories during this reset. When bit 7 (URST) is set to '0' the actions in the sequencer memory will be performed starting from address $FA02_{16}$ The DIP executes the instructions stored in sequencer RAM at a clock rate of 1.152MHz.

DIP instructions <U_INT0>, <U_INT1>, <U_INT2>, <U_INT3> and <U_VINT> <X> generate a DIP interrupt to the CR16B. The corresponding interrupt vector can be read from register DIP_CONTROL_REG[3-0]. <U_VINT> <X> set bits 3 to 0 to value <X>

If the prescaler mode bit is set to 1 and the DIP executes the U_PSC command the SCLK is divided by 16. This clock division remains active after the U_PSC command is executed until the DIP executes a <U_INTx> or <U_VINT> command or the prescaler mode bit is set to 0.

The break interrupt bit in the DIP control register is set by the DIP if the BRK command is executed. At this time also a DIP interrupt is generated at the CR16B. After execution of the break command the DIP program counter is not incremented until a 1 is written to the break interrupt bit. The CR16B can read the program counter from the time the BRK command is executed until the break bit is cleared.

Table 4: DIP Commands overview

Command	OPCODE	Description
BR	0x1	Branch Always
BRK	0x6E	Break for CR16B
JMP	0x2	Jump to subroutine (4 deep)
JMP1	0x3	Jump conditionally to subroutine
RTN	0x4	Return from subroutine
WNT	0x8	Wait until start of timeslot(s)
WT	0x9	Wait N time symbols
WSC	0x48	Freeze slot counter and wait for 8 kHz sync on STR0 to continue.
RFEN	0xB	Enable RF clock
RFDIS	0xA	Disable RF clock
BK_A	0xE	Set memory bank for ADPCM chan 0
BK_A1	0x5	Set memory bank for ADPCM chan 1
BK_C	0xF	Set memory bank for burst mode controller, micro wire and encryption unit

Table 4: DIP Commands overview (Continued)

Command	OPCODE	Description
SLOTZERO	0xD	Reset internal CLK100 timer
EN_SL_ADJ	02C	Enable DECT bitclock phase adjustment
WNTP1	0x7	Increment symbol counter
WNTM1	0x6	Decrement symbol counter
LD_PTR	0xC	Load pointer for indirect Data Ram access
UNLCK	0x28	Enter “PP unlocked” mode
A_RX	0x49	Select ADPCM buffer to receive B_fields.
A_TX	0x4A	Select ADPCM buffer to transmit B_fields.
A_MUTE	0xC1	Set Mute on ADPCM channel 0
A_MTOFF	0xC9	Set Mute off ADPCM channel 0
A_MUTE1	0xCA	Set Mute off ADPCM channel 1
A_MTOFF1	0xCB	Set Mute off ADPCM channel 1
A_STOFF	0xC2	Set Sidetone off ADPCM channel 0
A_STON	0xCC	Set Sidetone on ADPCM channel 0
A_RCV<X>	0x80-0x8F	Set Receive level for ADPCM ch 0
A_NORM	0xC5	Set ADPCM chl 0 to normal mode
A_RST	0xC0	Reset ADPCM channel 0
A_RST1	0xEB	Reset ADPCM channel 1
A_LDR	0xC6	Initialise start of ADPCM channel 0 read buffer
A_LDR1	0xCE	Load ADPCM channel 1 read address
A_LDW	0xC7	Load ADPCM channel 0 write address
A_LDW1	0xCF	Load ADPCM channel 1 write address
B_TX	0x31	Transmit any data from Data Ram
B_ST2	0x21	Transmit fixed ETSI S-field in PP or FP mode
B_AT	0x32	Transmit A-field
B_AT2	0x37	Transmit A-field and A-field CRC (R_A)
B_BT	0x34	Transmit B-field

Table 4: DIP Commands overview (Continued)

Command	OPCODE	Description
B_BTFU	0x25	Transmit full slot unprotected B-field, B-field CRC (X) and Z-field (Z)
B_BTFP	0x35	Transmit full slot protected B-field, B-field CRC (X) and Z-field (Z)
B_BTDU	0x71	Transmit double slot unprotected B-field, B-field CRC (X) and Z-field (Z)
B_BTDP	0x72	Transmit double slot protected B-field, B-field CRC (X) and Z-field (Z)
B_SR	0x29	Receive S-field
B_AR	0x3A	Receive A-field
B_AR2	0x3F	Receive A-field and A-field CRC (R_A)
B_RON	0x2F	Transmit A-field CRC or Receive and compare A-field
B_RINV	0x2E	Invert last bit A-field R_CRC
B_BR	0x3C	Receive B-field
B_BRFU	0x2D	Receive full slot unprotected B-field, B-field CRC (X) and Z-field (Z)
B_BRFP	0x3D	Receive full slot protected B-field, B-field CRC (X) and Z-field (Z)
B_BRDU	0x79	Receive double slot unprotected B-field, B-field CRC (X) and Z-field (Z)
B_BRDP	0x7A	Receive double slot protected B-field, B-field CRC (X) and Z-field (Z)
B_XR	0x2B	Receive X-field
B_WB_ON	0x65	Write zeroes in B-field receive buffer if A-CRC is ‘0’
B_WB_OFF	0x64	Disable B_WB_ON command
B_WRS	0x39	Write BMC status information to Data Ram
B_RC	0x33	Load BMC control information from Data Ram in BMC
B_RST	0x20	Set BMC in power down mode.
B_XT	0x24	Transmit X-field

Table 4: DIP Commands overview (Continued)

Command	OPCODE	Description
B_XOFF	0x26	Deactivate B-field X_CRC
B_XON	0x27	Activate B-field X_CRC
C_LD	0xFA	Reserved
C_ON	0xEE	Reserved
C_OFF	0xEF	Reserved
C_LD2	0xBA	Load Codec 2 control bytes from Data Ram in Codec.
C_ON2	0xAE	Switch Codec 2 on.
C_OFF2	0xAF	Switch Codec 2 off.
D_LDK	0x50	Load encryption data from Data Ram in DCS unit
D_PREP	0x44	Preprocess encryption data in DCS
D_WRS	0x5F	Write current encryption status to Data Ram
D_LDS	0x57	Load intermediate encryption status from Data RAM
D_RST	0x40	Reset keystream generator
D_ON	0x42	Enable DSC
D_OFF	0x43	Disable DSC
M_WR	0xB9	Transfer from Data Ram to MEN1n
M_RST	0xA9	Stop command M_WR
M_INI0	0xA0	Set SK,SO start/end levels to 0, SK falling edge
M_INI1	0xA1	Set SK,SO start/end levels to 1, SK falling edge
MEN1n	0xA4	Reset pin MEN1n to 0
MEN1	0xA5	Set pin MEN1n to 1
P_EN	0xE9	Enable PD pins from 3-state to active 1
P_LDH	0xED	Set marked PD pins to '1'.
P_LDL	0xEC	Set marked PD pins to '0'.
P_LD <n>	0xE8	Set PD pins to <n>
P_SC	0xEA	Synchronise to LCK pin and/or S-field detect
U_INT0 U_INT1 U_INT2 U_INT3	0x61, 0x6B, 0x6D, 0x6F	Generate interrupt to CR16B
U_PSC	0x60	Set CR16B SCK prescaler to 16
U_VINT <x>	0x63	Generate Vectored interrupt 0-F, FF

For more detailed information see the SC14424 DECT Family Commands Manual.

4.5 THE RADIO FRONT-END INTERFACE

The SC14424 can fully comply to any radio interface (including ARi1™* providing all necessary timing signals and control information.

4.5.1 Synthesizer interface (MICROWIRE)

A flexible serial interface allows the user to control almost any RF synthesizer device. Any number of bits can be transferred, one enable pin MEN1n, (pin # 23) is programmable to have an active low or high level. The serial interface consists of a data output (SO, pin # 24) and a clock (SK, pin # 25). The data rate is 1.152 Mbit /s. Data from the data memory to this interface is transferred using DIP command <M_WR>. Transfer can be stopped after with command <M_RST>. The initial and final polarity and active edge of SK and SO can be set once with the commands <M_INI0> <M_INI1> as shown below.

Table 5: M_INI0, M_INI1 commands

Command	Description
Startup values (RSTn = 0)	SK start/end level = 0, SO data clocked out on falling edge of SK, SO start/end level = 3-state, can be pulled high or low with external Resistor. SO polarity during transmission can be inverted in RAM
M_INI0	SO, SK start/end level = 0. SO data clocked out on rising edge of SK. SO polarity during transmission can be inverted in RAM.
M_INI1	SO, SK start/end level = 1. SO data clocked out on rising edge of SK. SO polarity during transmission can be inverted in RAM.

The RFCLK (pin # 12) output pin on the SC14424 can be used as the reference input clock for the synthesizer. This clock is a buffered output of the frequency controlled crystal oscillator of the SC14424 running at 10.368 MHz (9x DECT bit clock). For power saving it is possible to enable or disabled the RFCLK output with DIP commands RFEN and RFDIS.

* ARI™ is a trademark of National Semiconductor Corporation

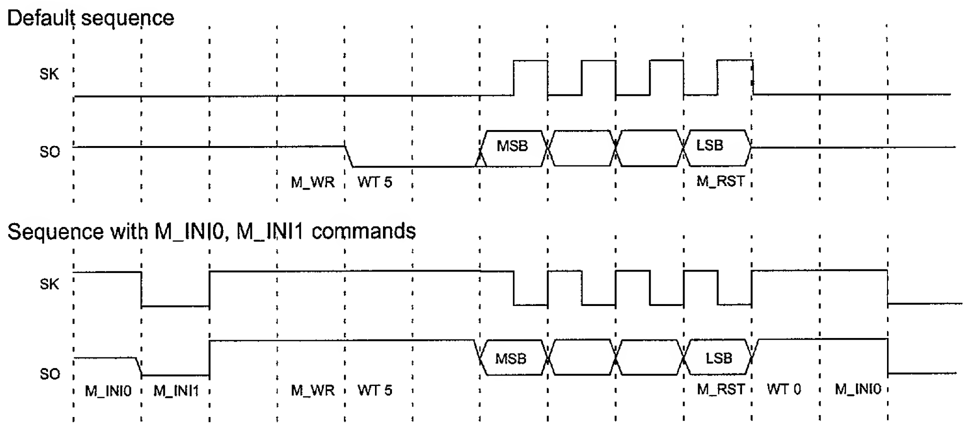


FIGURE 11. MICROWIRE timing diagram

4.5.2 Programmable control pins

The SC14424 provides eight programmable timing signals PD[7:1] (pin # 2..8) and PD0 which is internally connected to the peak hold RSSI. Each of them can be individually set or reset at any time during a frame using DIP commands <P_LDH>, <P_LDL> or <P_LD> <n>. These timing signals can be used to activate or deactivate the front end circuitry. Three timing signals PD5, PD6 and PD7 have a 12 mA output drive capability for applications such as driving PIN diode switches.

After reset the PD outputs will be in the Hi-Z mode. Only when enabled with the P_EN command the pins will get their programmed value. This allows to control with external resistors these pins to be high or low after reset.

4.5.3 RSSI peak hold ADC

In order to select the best frequency channel with respect to signal to noise ratio, the so called Received Signal Strength Indication (RSSI) is measured for the different frequency bands.

The on-chip peak hold 6-bit ADC can be used to convert the RSSI peak value on pin RSSI (pin # 19). The peak detector can track peaks from zero to maximum scale within 32 microseconds. To extend the dynamic range an external resistor divider network should be used. Using DIP command <B_WRS>, the ADC data bits can be written into the Data memory at different locations for each slot.

The timeslot to measure the RSSI level is determined by PD0, which is internally connected to the gate of the peak hold ADC. As long as PD0 is low, the peak value is measured. Whenever PD0 is high the ADC input pin is connected to ground to discharge the external capacitor.

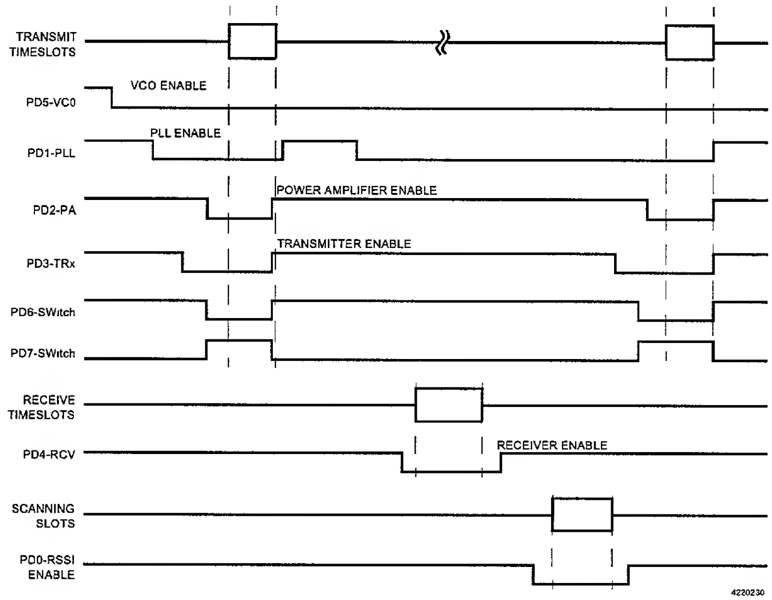


FIGURE 12. Typical timing on radio frontend interface

4.5.4 Modulated output

The modulation method for RF transmissions in DECT is gaussian frequency shift keying with a bandwidth x bit period product, BT=0.5. The SC14424 generates at the Transmit Data Output (pin TDO, pin # 22) the burst data at the baud rate (1152 kbit/s). The TDO output can be programmed to output a gaussian shaped symbol. The shape is spread over three symbols and coded with an eight bit DAC. The amplitude can be controlled with another 6 bits. The Gaussian output voltage is independent of the supply voltage level. With information loaded in the Data memory this output can be controlled. With control bit "INV_TDO" the TDO output can be inverted. With M[1:0] set to: M[1:0]='00' Digital output is selected. M[1:0] ='10' powers down. M[1:0]='01' activates the gaussian output shape. M[1:0]= '11' set TDO to the mid level. With VOL[5:0] the amplitude of the gaussian shape can be trimmed step wise.

4.5.5 Demodulated data input

The demodulator in the RF front end regenerates the data bits, when activated by one of the timing signals PD[7:0], the data bits. The Received Data In (RDI, pin # 20) is clocked into the SC14424 with the internally regenerated bitclock. With control bit "INV_RDI" inversion of RDI signal can be selected.

The SC14424 is equipped with a very stable and accurate received symbol timing extraction unit using a nine times over sampled digital phase correlator on the S-field. A fast (total delay of less than 30 nsec>, low power (<500 µA when active) comparator allows for demodulated data to be input on the RDI pin, with input levels typically as low as 100mVpp.

4.5.6 DC offset compensation

To allow for compensation of the DC offset generated in the RF circuitry due to mixer imbalances and/or frequency offsets, the SC14424 offers two solutions. The first solution uses the S-field bit sync pattern to measure the DC-offset by means of measuring the eye opening duty cycle. DC offset can only be measured correctly if the comparator reference level is within the eye opening of the received data input. Four symbols are measured with nine times oversampling. At the end of each received packet the measured offset is stored in the Data RAM status information bytes The CR16B can control a 6-bit DAC to compensate for the DC-offset. The DC offset value ranges from 0 to 36, binary coded. If the output value equals 18 then there is no DC offset. In case the output is:

$$0 \le \text{output} \le 17$$

Then the DC offset of the data signal is positive and the reference level should be adjusted accordingly.

If the output is:

$$19 \le \text{output} \le 36$$

then the DC offset of the input data signal is negative and the reference level should be lowered accordingly. In the MAC "locked" state (S and Qt detected) the DC offset is reported as zero if the S-field is incorrectly received. In the "unlocked" state the DC offset value is continuously updated and allows for initial DC offset control.

A second DC offset method is implemented to be used in case the offset variation exceeds the received signal eye opening. The SC14424 provides an accurate control pin PD1 in case the DC offset is measured with an external

capacitor. One can program the PD1 pin to rise or fall synchronised with the end of the bit sync pattern of the S field or the end of the complete S field.

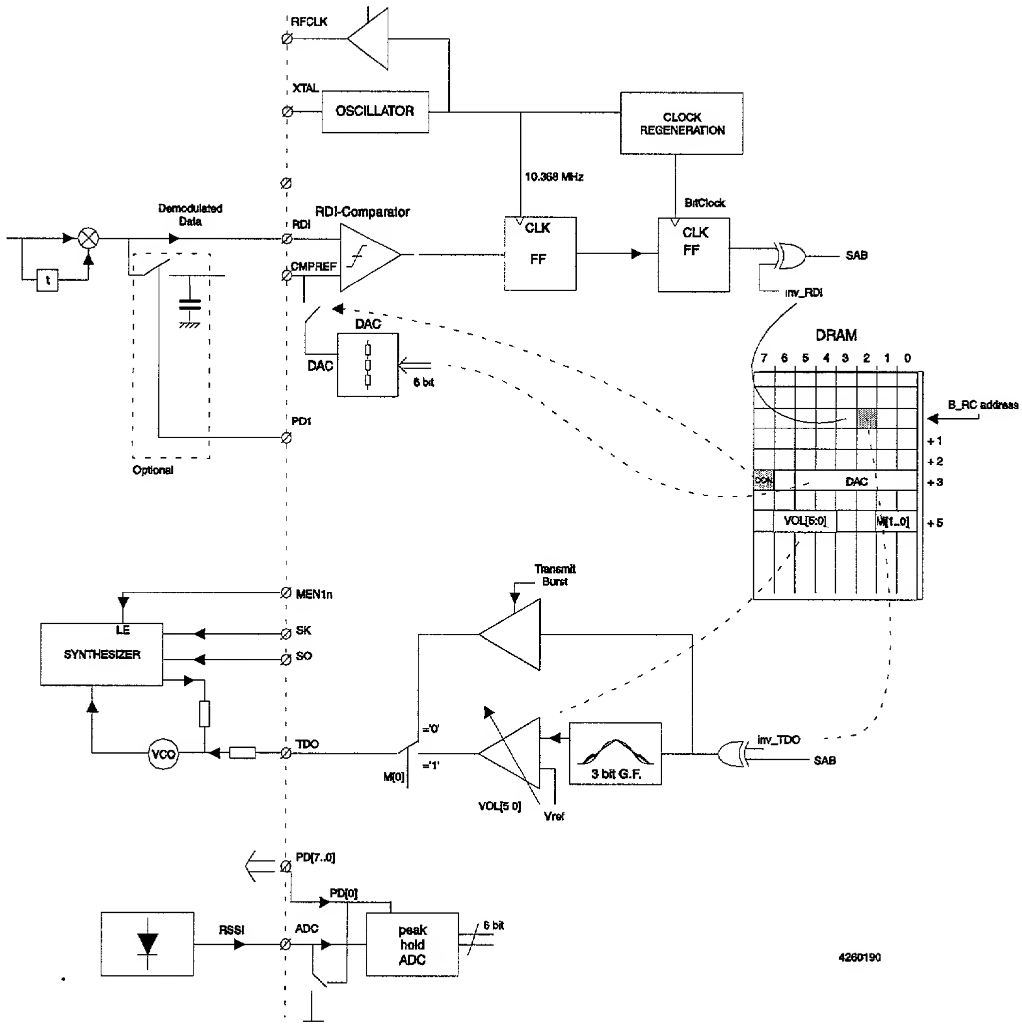


FIGURE 13. SC14424 Radio frontend interface

4.6 ECP/CODEC INTERFACE

The SC14424 has a very flexible digital interface to external codecs, ISDN interface circuits and serial data interfaces. Figure 14 shows the ECP/CODEC interface. The interface allows access to channels B1 and B2. Depending on the selected format as shown in Figure 15, channel B1 or B2 carries various combinations of PCM coded (u-Law or A-law or linear) data, external codec data or 16 bits transparent data for data applications. Channel B3 is connected to the on-chip codec 2 and can not be accessed externally.

The input data of all three channels are directly stored in fixed ECP RAM locations (E.g. b1lawin contains pcm codec "u/A-law" samples of channel b1 used in ECP formats 0,1,2 and 6.)

The output data are indirectly accessed through the ECP switch table. (E.g. RAM[swb1out] means that switch table location swb1out contains the pointer to a ram location that hold data to be output on timeslots "ram word 1" or "16 bits linear" of channel b1).

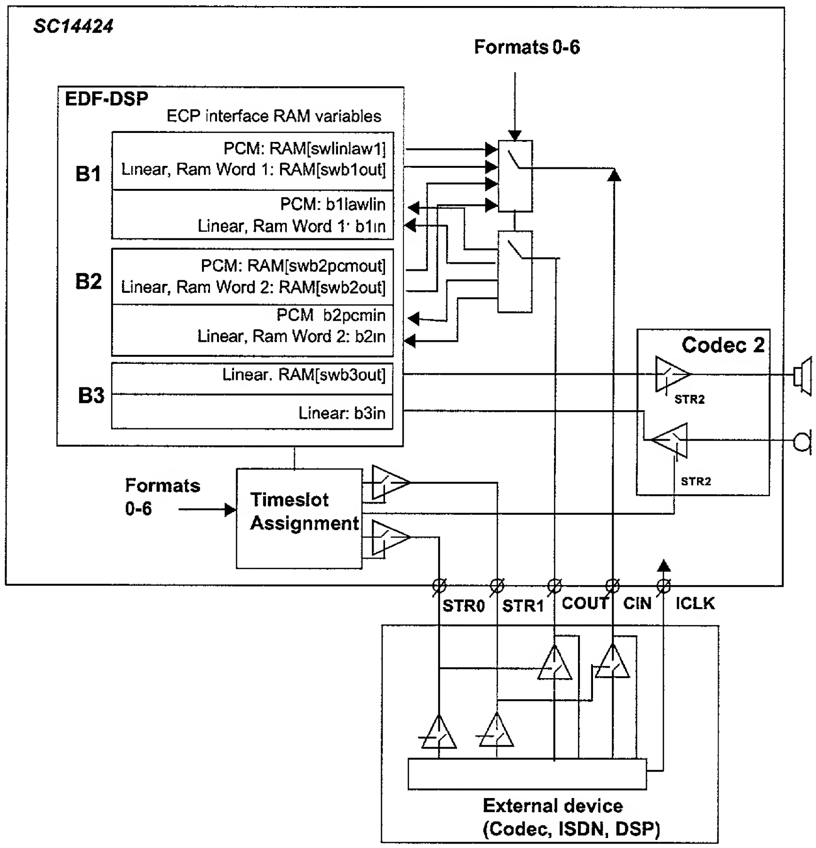


FIGURE 14. ECP/Codec interface

The interface has the following interface signals:

- CIN/COUT. Bidirectional data signals. The direction depends on the format that is selected. COUT is an open DRAIN output.
- STRO/STR1 are the input/output enable signals. If high, data on CIN/COUT are clocked in and out the SC14424 with ICLK. If master formats are selected (formats 1, 4, 5) then STR0 and STR1 are always output. In all slave formats STR0 must be high for at least two ICLK cycle and at least one ICLK cycle must be applied between the falling edge of STR0 and the rising edge of STR1 and between multiple strobes like in format 3.
- ICLK is the data clock. ICLK may be divided by two and can be provided externally or generated internally. (see Table 19). A 2.304 MHz or 1.152 MHz clock is output on ICLK if generated internally. Data on CIN, COUT, STR0 and STR1 is clock out on the rising edge and latched on the falling edge of ICLK. The external clock must be a multiple of 8 kHz upto 2048 kHz or 4096 kHz in case div 2 option is selected. The repetition rate of STR0 must be 8 kHz. To prevent data from being lost frequency and phase synchronisation must be performed using DIP <WSC> command and DAC output to tune the SC14424 Xtal frequency.

If master formats are selected (Formats 1, 4, 5) then ICLK is always output. In slave formats ICLK is input if ECP_CONTROL_REG_1.bit1 is 0 else ICLK is an output.

4.6.1 Formats

The ECP/Codec interface has the following formats which can be set by programming ECP control register 1 (see Table 6):

Format 0 (default after reset)

Format 0 is used to interface to ISDN ICs. STR0, STR1 are input signals. Both B1 and B2 data are coded according to A-law or μ-Law and on both channels echo suppression is performed. The second block of 16 bits is transferred transparently to/from RAMword2 if STR1 is extended. This information block gives a 128kbit/sec channel for data services or handle IOM-2 monitor, command and indication channels. To support a clock rate at double the bit rate, the ICLK bit must be set to 1.

Format 1

Format 1 is used to interface to both the external codec (B2) and a 64kbit/s speech channel (B1). STR0 and STR1 are both output signals. B1 is coded according the A-law or μLaw, B2 is coded linearly: 14 bit two's complement sign extended to 16 bit. On channel B1 echo suppression is performed and on channel B2 echo cancelling and suppression is performed. To program the codec refer to Table 9.

Format 2

Format 2 is used to interface to two external 64kbit/s channels. STR0, STR1 are input. Both B1 and B2 data are coded according to A-law or μLaw and on both channels echo suppression is performed. The second timeslot of 16 bits on STR1 is transferred transparently to/from RAMword2.

Format 3

Format 3 is used for four transparent 64kbit/s connections over DECT. STR0, STR1 are input signals. STR0 must be continuous with an 125 μsec repetition time. STR1 may consist of multiple timeslot assignment strobes. If STR0 is high, data transferred transparently to/from RAMword1, during STR1 data is transferred transparently to/from RAMword2. No further data processing to be done on this channel. With the 8kHz interrupt source (CLK8k_INT) enabled, 8kHz synchronous data processing by CR16 can be performed.

Format 4

Format 4 is equal to format 1 except that data on B1 is 14 bits two's complement sign extended to 16 bits. This format is useful with an external DSP.

Format 5

Format 5 is intended for connection of an external DSP performing processing on B1 and B2, 14 bits two's complement sign extended to 16 bits. The second timeslot of STR1 is not supported. Optionally echo suppression can be performed on the two channels.

Format 6

This format is equal to format 0 with the exception that STR1 can vary from 0 to 16 bits. Only if STR1 is high data is clocked in and out to/from RAMword2. B1 and B2 are μ-law or Alaw. On both B1 and B2 echo suppression is performed.

The internal codec is not configured through any of the ECP formats. The codec is mapped to channel B3, (see Figure 14)

4.6.2 External synchronisation

The SC14424 enables synchronisation to the incoming 8 kHz in all formats were STR0 is input. Both the crystal frequency and the DECT frame phase can be tuned. After (soft) reset the SC14424 internally generated 8 kHz which is synchronised by STR0 input pin. The time difference between the STR0 and the internal 8 kHz signal is measured in units of the bit clock (870nsec in case of 1.152 MHz, 435nsec in case of 2.304 MHz) and the result is stored in RAM location $FBFF_{16}$. In master mode value 0 is stored. In slave mode value $5B_{16}$ (Div 1) or $2D_{16}$ (Div 2) is stored. The value must be kept constant If the value changes, crystal frequency must be adjusted by tuning the crystal via the DAC output. See also chapter 4.10.1. If the frequency is not adjusted, samples might get lost or duplicated, but they will not be corrupted.

DIP command <WSC> halts the TDMA co-processor. The next DIP instruction is executed 184 symbols after the first rising edge of the STR0 input signal. This allows to synchronise the 10ms DECT frame to an incoming 8 kHz signal at any bit position. If no external synchronisation is performed, data is still transferred over the ECP interface, but data might get lost, either repeated or deleted.

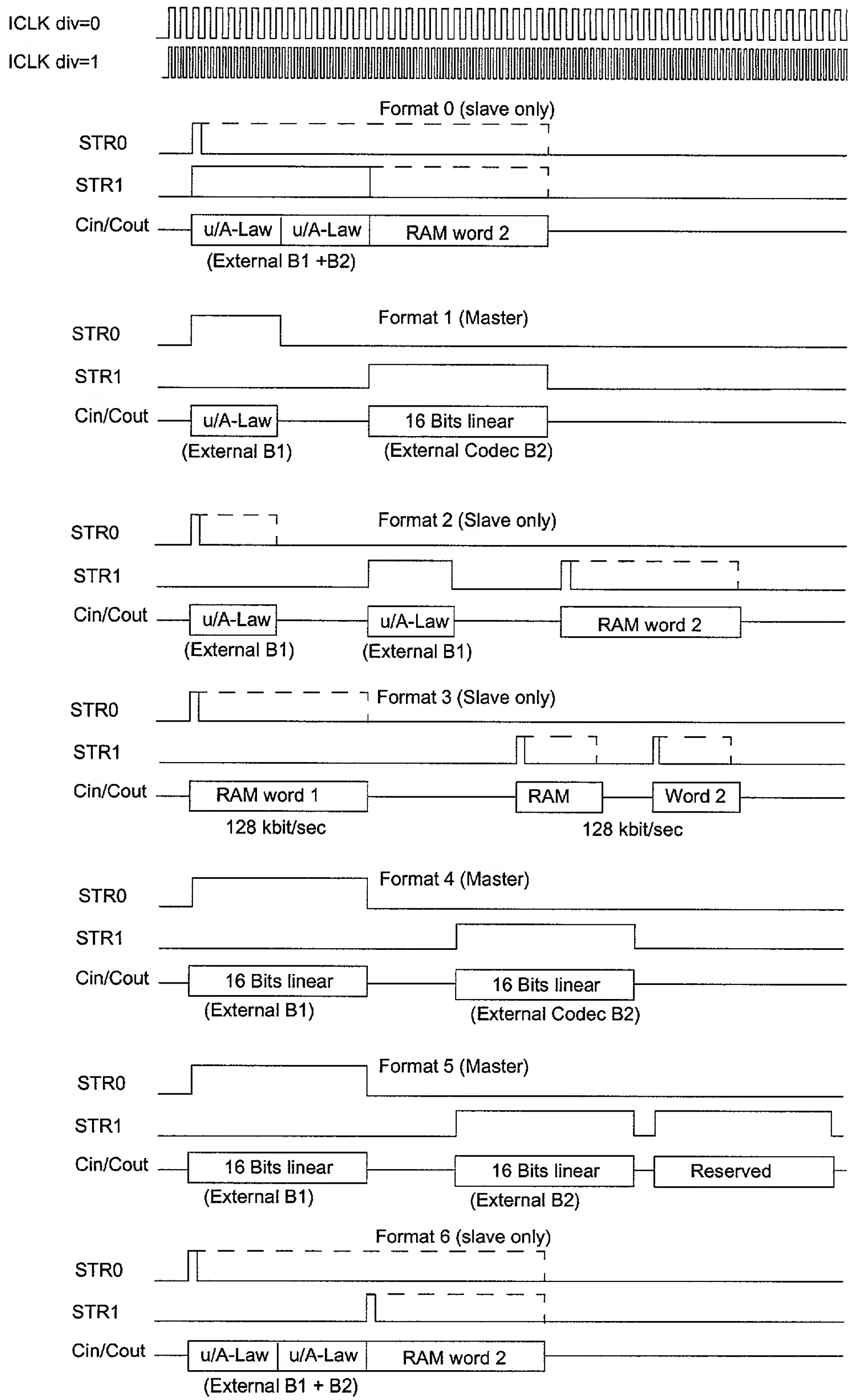


FIGURE 15. ECP interface formats

4.7 EMBEDDED DEDICATED FLEXIBLE DSP

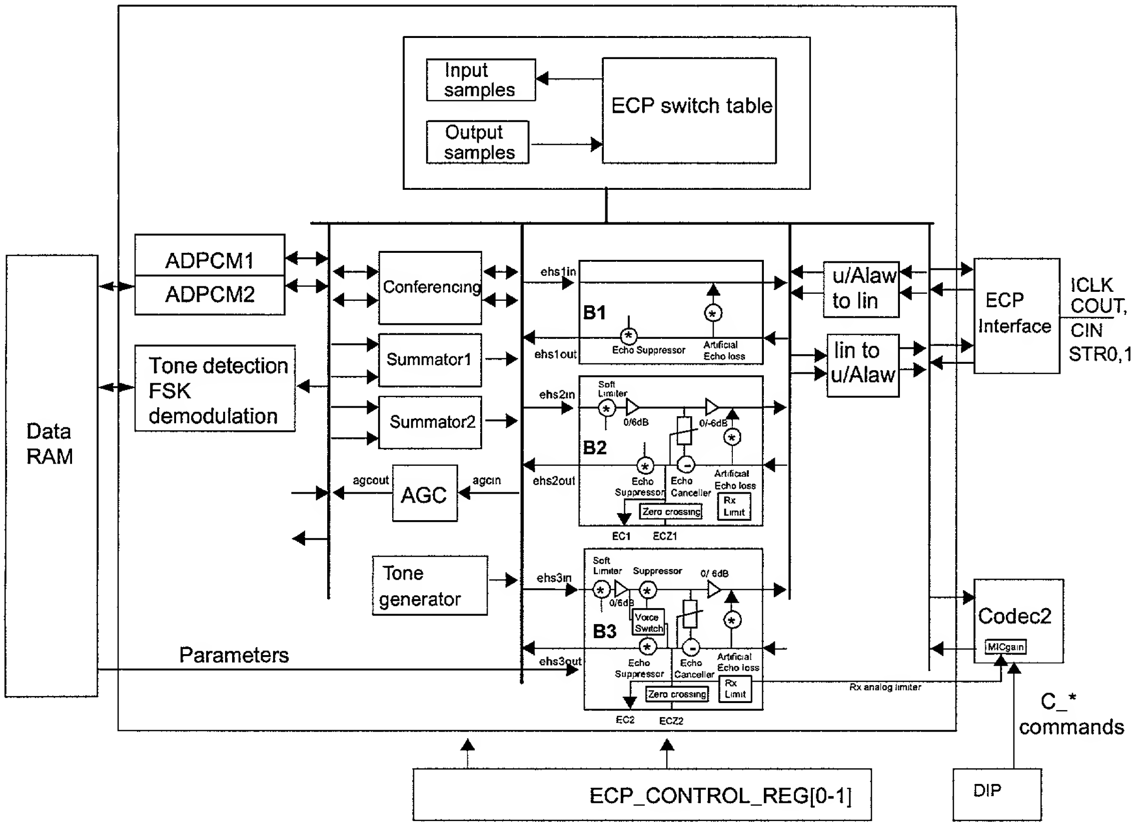


FIGURE 16. EDF_DSP Functional diagram

The 14424 has an embedded dedicated flexible DSP (EDF_DSP) which can execute the following functions as shown in (see Figure 16):

1) 2 channel ADPCM transcoding
2) Dual Tone generation (DTMF)
3) 2 channel u-law/Alaw conversion
4) 2 channel Echo cancelling
5) 2 channel Echo suppression
6) 2 channel Soft limiting
7) 2 channel Centre clipping
8) 4 channel conferencing.
9) Automatic gain control (AGC)
10) FSK demodulation for Caller-id (V23 and Bell 202)
11) 11 individual Tone detectors (DTMF, CAS, FAX)
12) Half duplex handsfree
13) Listening-in

The data flow between the functional blocks is fully programmable through the **ECP switch table.** The outputs of any of the functional blocks can be routed to any of the inputs of others blocks. This gives a high degree of flexibility.

The **modes** of the EDF_ECP individual functions can be programmed via **ECP_control_register[0-1].** The **parameters** of the functions, like attack and decay times are programmable via the **data RAM**.

Also the processed **data samples**, either ADPCM or transparent modem data, is automatically stored in **data RAM** at programmable locations with automatic pointer increments.

4.7.1 ADPCM transcoder

The SC14424 has two full duplex ADPCM transcoders which encodes/decodes 14 bits linear codec voice samples down to 32 kbit/sec. The 32kbit/sec ADPCM transcoding is fully compliant to G721/G726 and is used for normal voice transmission.

Muting

The SC14424 can use the correctness of the A-field CRC to determine B-field repetition by setting the SENSE_A (see table 18) bit to '1'. If an erroneous frame is received the new B-field will not be written and the last received B-field will be repeated in order not to disturb the ADPCM sound.

If the SENSE_A bit is kept to '0' and an A-field error is detected, the CR16B can also decide to initiate a smooth mute on either channel 0 or 1 with the <A_MUTE> or <A_MUTE1> commands.

If the SENSE_S bit is set, no B-field data is written if the BMC lost synchronisation (IN_SYNC = '0').

Volume control

The signal level on ADPCM channel 0 can be set from 0 to -36 dB in steps of 3 dB with the <A_RCVx> command.

4.7.2 Tone generators

The SC14424 has two general purpose tone generators. In addition the eleven tone generators that are used by the tone detectors can be routed to any of the DSP inputs.

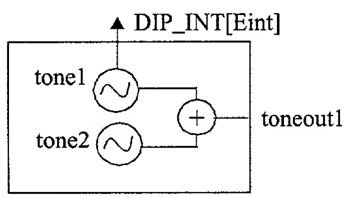


FIGURE 17. Tone generator

The lower and higher tone frequencies as well as volume of both general purpose generators can be set by initialising the parameters. The summed output can be attenuated with Atttone1, Atttone2 parameters to two individual outputs tone1 and tone2

The cadence of the DTMF tones can be programmed by presetting DTMFpreseton which determines the on-time and DTMFpresetoff which determines the off-time. If the ONOFFCOUNTER is started it will automatically be loaded with value DTMFpreseton. If the counter expires, a DIP[ECP_INT] interrupt will be generated, DTMFpresetoff is loaded and the counter is restarted automatically. The interrupt routine can reprogram a new frequency. If the counter expires again, DTMFpreseton is reloaded again but no interrupt is generated.

4.7.3 Echo cancellers

The SC14424 has two Near End Echo Cancellers (NEC) that cancel echoes introduced in the line interface hybrid. (see Figure 18). The EC algorithm uses a 32 tap FIR filter with the commonly used Least Mean Square (LMS) update algorithm. The coefficient update constants *($ECmu_n$)* and the coefficients *(EC_C_i)* are stored in the Data RAM and can be initialized and monitored during operation. A Voice Activity Detection (VAD) algorithm is implemented to perform Echo suppression with a programmable attenuation and a smoothly switching on/off characteristic. The implemented algorithm incorporates all necessary means to allow for fast convergence, prevents incorrect update of the coefficients and switches on or freezes the echo canceller/suppressor in case the receive level has a certain ratio over the transmit level. The EC on/off control has programmable time constants. Two different time constants for switching on and off exist.

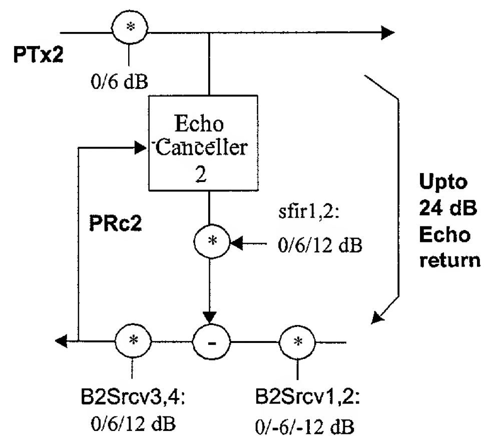


FIGURE 18. Echo cancellers

Echo canceller coefficient-update-constant ($ECmu_n$) and transmit and receive levels time-constants depend on the mode.

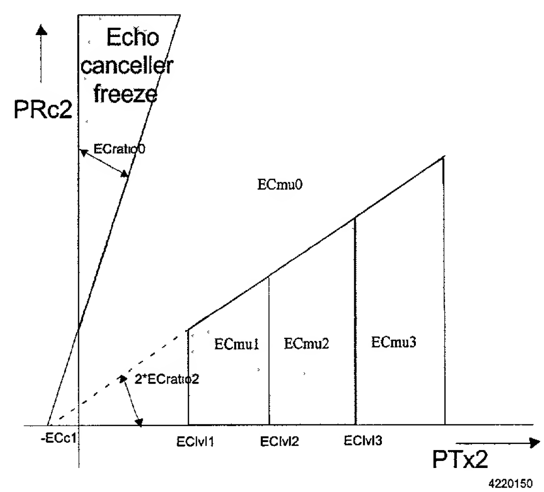


FIGURE 19. Echo canceller modes

Different modes are selected depending on the ratio between receive and transmit levels.

If $P_{TRX}/P_{RCV} \leq$ *ECratio0* then the echo canceller is frozen.

In all the other situations the echo canceller update constant $ECmu_n$ gets a value dependent on the ratio of the transmit and receive level.

If $P_{TRX}/P_{RCV} \geq ECratio0$ *and* $P_{TRX}/P_{RCV} \geq ECratio2$ *then* ECmu0 is selected.

If $P_{TRX} \geq EClvl1$ and $P_{TRX}/P_{RCV} \leq ECratio2$ then ECmu1 is selected.

If $P_{TRX} \geq EClvl2$ and $P_{TRX}/P_{RCV} \leq ECratio2$ then ECmu2 is selected.

If $P_{TRX} \geq EClvl3$ and $P_{TRX}/P_{RCV} \leq ECratio2$ then ECmu3 is selected.

4.7.4 Echo suppressors

The echo suppressors (ES) suppresses the echoes of the transmitted signal with programmable attenuations, thresholds, ratios and time constants. (see Figure 20)

Switch on and off times as well as suppression levels are programmable for both channels. (x = 1,2)

The actual suppression factors SPsup1 and SPsup2 can be read from Data ram.

A time delay (SPCNTINI) can be programmed to delay the ES to turn off. If the EC switched on, threshold SPCNTMN determines whether the EC switches off with normal time constant or switches off with an extra time delay.

4.7.5 Centerclipper

Both echo suppressors have a centerclip function:
If PRc1,2 < Centclip1,2 then the rcv signal will be suppressed with attenuation factor Centcatt.

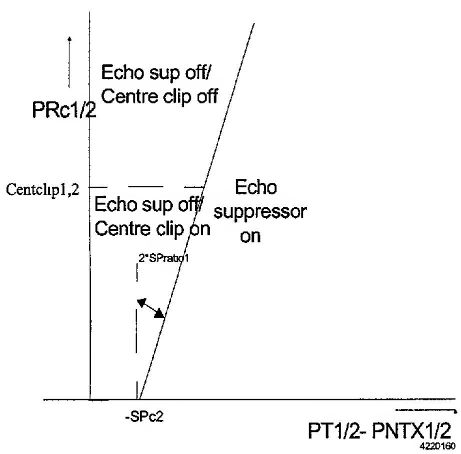


FIGURE 20. Echo suppressor modes

4.7.6 Soft limiter

The soft limiter attenuates the signal from the handset with if Ptrx > LVL4. Switch on and off times as well limit level are programmable for channels B2 and B3.

The actual limit factor SLlimit can be read from Data ram

4.7.7 Automatic Gain Control (AGC)

The AGC is used in conjunction with an external telephone answering machine IC. Figure 21 shows a typical TAM configuration with AGC. The Rxgain and Txgain must be subtracted from the overall gain to determine the AGC gain. The AGC can be set in the ECP_CONTROL_REG_x to +6/+12 dB. To increase the AGC gain, the AGC function can be cascaded in both receive and transmit direction. For typical application however the AGC is only used in the receive path.

Signals at agcin below LVL5 are amplified with 6/12 dB to agcout. Signal above LVL5 are limited to LVL5. (Figure 22) by reducing the gain.

The delay time constants to switch on and off are determined by TAGCon and TAGCoff.

The AGC can be switched off by excluding AGC signal path from the switch table.

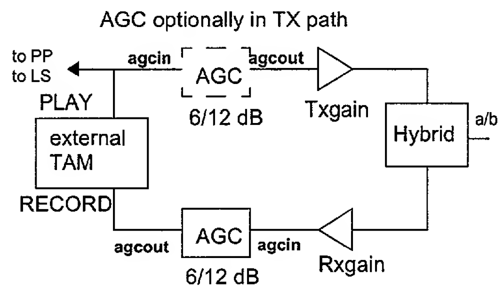


FIGURE 21. External TAM with AGC configurations

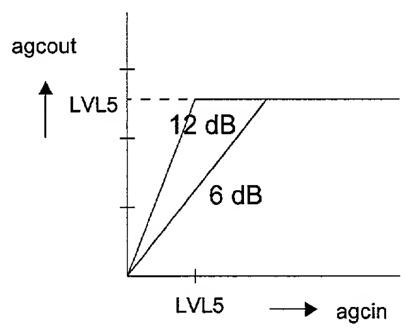


FIGURE 22. AGC gains

The AGC function comprises has gain stage which maximum gain is programmable with Sagc.

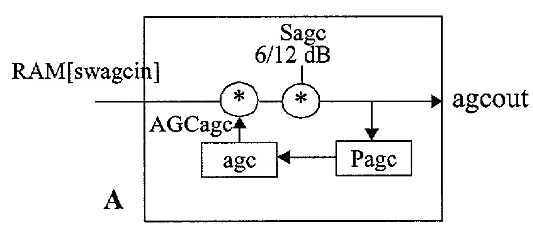


FIGURE 23. AGC functions

The actual AGC gain can be read from Data ram.

4.7.8 Voice activity and noise detection

The Voice Activity Detection (VAD) controls the echo canceller, the echo suppressor and soft limiter. It determines the level of the speech sources HS1 (PTx1), HS2 (PTx2), HS3 (PTx3), B1 (PRc1), B2 (PRc2) and B3 (PRc3). In order to minimise the effect of background noise, two additional noise level integrators can generate an offset for the speech levels. Their time constants are independent from the speech levels.

In order to prevent divergence in the echo canceller, fast changing signals from the handset will directly bypass the rise time.

4.7.9 Signal attenuation and conferencing

The SC14424 has programmable attenuations for all signal paths. The attenuation for the signals coming from chs1in and chs2in can be set with the parameters AttHS1 and AttHS2. The attenuation for the signals coming from B1 or B2 can be set with the parameters AttB1 or AttB2.

By setting one or more attenuation factors to 0, upto four multi party conferencing is possible (Example: two handsets, the an external Codec to external line and the "base station corded phone via Codec 2.)

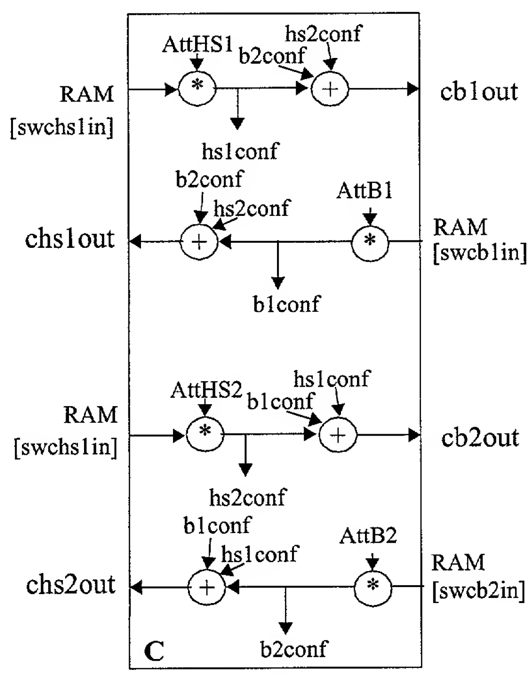


FIGURE 24. Conference function

4.7.10 Summators

The SC14424 has two general purpose summators that can be used to merge tone outputs to voice links to handset or line. The programmable attenuation of the summator gives flexible level control.

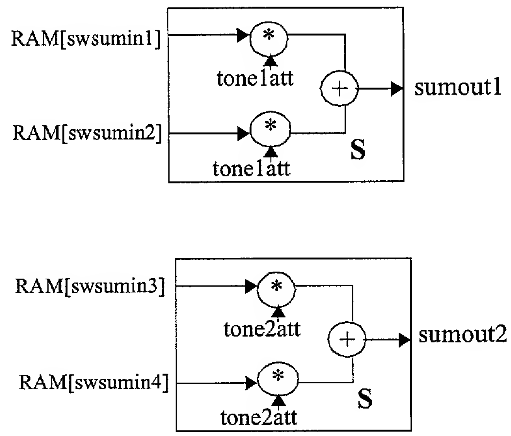


FIGURE 25. Summators

4.7.11 Side tone/Artificial echo

The SC14424 can add an artificial echo or side tone from the signal received from the line to signal transmitted to the line. For both B1 and B2 channel this echo is programmable with values AEL1att, AEL2att and AEL3att. The echoes are switched off if the values are 0.

4.7.12 PCM transcoders

The SC14424 has two PCM uLAw/A-law encoders/decoders according to ITU-T G.711. In ECP interface formats 0,1,2 and 6 the PCM data from B1 and B2 must be routed through the encoders via the switch table. In data mode linear samples from the internal codec 2 must be encoded. The PCM coder on channel B2 is only active if the ECON bit in the ECP_control_register is 0, else the echo canceller on B2 is active.

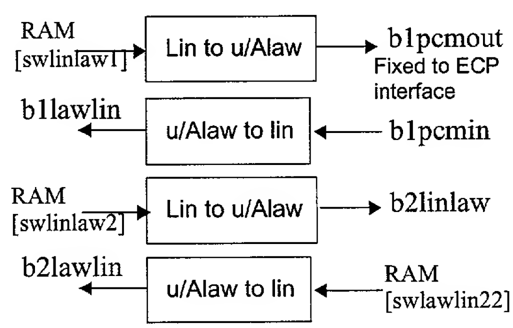


FIGURE 26. PCM encoding/decoding

4.7.13 Data mode

The SC14424 supports 64kbit/sec data mode for modem and fax applications. To configure the data mode the internal codec data should be routed through the u/ALaw or Alaw coder. The CLK8K_INT interrupt routine copies every 125 usec the PCM coded data to 2 full or one double slot unprotected or protected B-fields in data RAM.

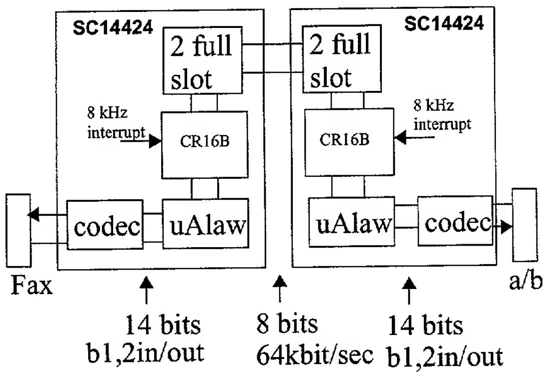


FIGURE 27. Data mode using PCM encoding

Transparent data mode with external devices can always be done in formats 3 using RAMWORD1 or RAMWORD2.

4.7.14 Caller-id

Caller-id for one of the two external lines is supported. On-hook caller-id (CID) data can be received on pin MiC2- which is connected to codec2 (channel B3). This pin can be selected in the CODEC control register. For off-hook caller-id on call waiting (CIDCW), data can be received via Mic2+ of Codec 2 (B3) and routed via echo canceller 2 to input RAM[swcidin] of the FSK, CAS and DTMF detector block.

Routing via the echo cancellers improves the talkdown performance of the detectors.

Tone detection

The SC14424 has eleven precision tone detector (see Figure 28) which are configured to simultaneously detect:

- One out of (4x4) programmable Dual Tone pairs.
- One (1x1) Tone Alert or CAS signal pair.
- 1 auxiliary single tone (E.g. Fax tone)

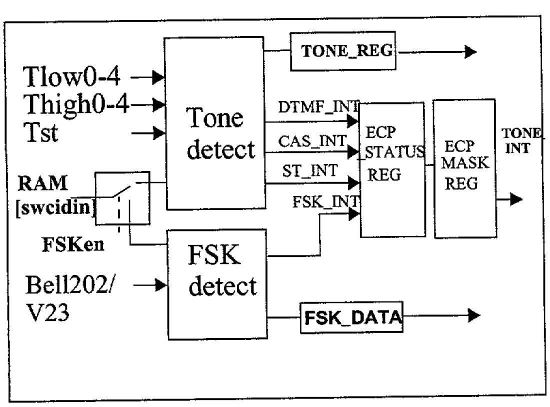


FIGURE 28. Tone and FSK detectors

The DTMF tones are in the range from 0-9, *,#, A-D and are used for remote control of the SC14424 over the telephone line. The CAS tone is a dual tone signal with frequencies 2130 and 2750 Hz used to initiate caller-id on call waiting.

To enable the CAS/DTMF/Single tone detectors bit FSKen must be set to 0 in the ECP_CONTROL_REG 1.

Any tone frequency is programmable (LOW1...HIGH5) as well as the sensitivity and tone duration. The tone detectors are paired.

As soon as a LOWn and HIGHn (n=1..4) both detect their programmed tone or as LOW5 and HIGH5 are both detected (in case of CAS tone), a counter starts to be incremented (with DTMFcntrinc in case of DTMF, CAScntrinc in case of CAS and STinc in case of single tone detection). When the counter reaches its maximum value, one or more interrupts flags DTMF_INT_P, CAS_INT_P or ST_INT_P will be set in the ECP_STATUS_REG and a TONE_INT will be generated. When the tone pair is not detected any more the counter starts to decrement (with DTMFcntrdec, CAScntrdec, STcntrdec). When the counter reaches its minimum value one or more interrupts flags DTMF_INT_N, CAS_INT_N or ST_INT_N will be set in the ECP_STATUS_REG and a TONE_INT will be generated.

The interrupts in the ECP_STATUS_REG must be cleared by writing a '0' to the ECP_STATUS_REG. TONE_INT must be cleared in the RESET_INT_PEND_REG2.

In order to improve the tone detection, the near end echo canceller is enabled during playback_speech and tone generation.

Table 6: ECP_TONE_REG

DTMF digit	Low Tone	High Tone	Binary value
1	flow1	fhigh1	10001000
2	flow1	fhigh2	10000100
3	flow1	fhigh3	10000010
4	flow2	fhigh1	01001000
5	flow2	fhigh2	01000100
6	flow2	fhigh3	01000010
7	flow3	fhigh1	00101000
8	flow3	fhigh2	00100100
9	flow3	fhigh3	00100010
0	flow4	fhigh2	00010100
*	flow4	fhigh1	00011000
#	flow4	fhigh3	00010010
A	flow1	fhigh4	10000001
B	flow2	fhigh4	01000001
C	flow3	fhigh4	00100001
D	flow4	fhigh4	00010001

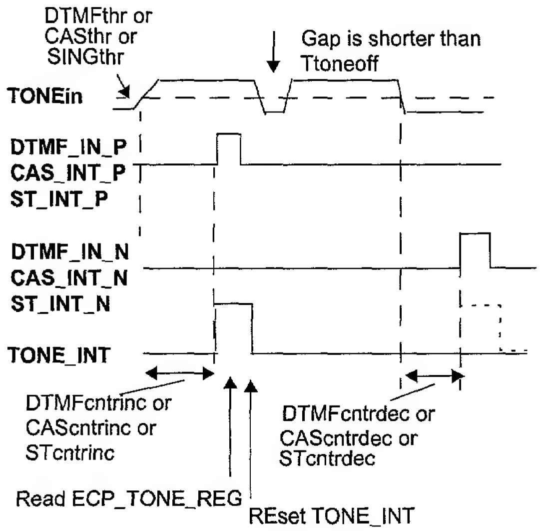


FIGURE 29. Tone detector timing

FSK detection

The SC14424 is able to detect on-hook caller-id information which is Frequency Shift Keying (FSK) modulated according to Bell-202 and V.23 standards. The FSK standard can be selected by programming different frequencies.

To enable the FSK detector, bit FSKen in the ECP_CONTROL_REG must be set to '1'.

The FSK detector always tries to find the MARK signal, thereby skipping the channel seizure signal. As soon as a 1 to 0 transition is found, it starts clocking in the 8 databits. When the stop bit is received an FSK_INT interrupt in the ECP_STATUS register is set. If the M_FSK_INT was enable before, the TONE_INT is also generated. (see Figure 30)

FSK_INT is cleared if the ECP_STATUS_REG is read. The TONE_INT must be cleared in the RESET_INT_REG_2. The received FSK byte can be read from register FSK_DATA. The mark and space bits are automatically removed by the receiver. The checksum evaluation shall be done by the CR16B.

The Carrier Detect signal (CD) and FSK raw data (RD) (start, data, stop bits) can always be read in DataRAM.

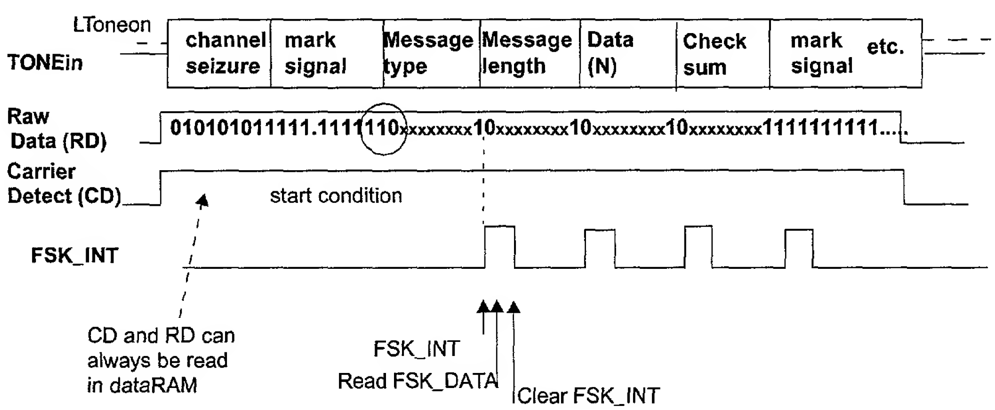


FIGURE 30. FSK detector timing

4.7.15 Speakerphone and listening-in

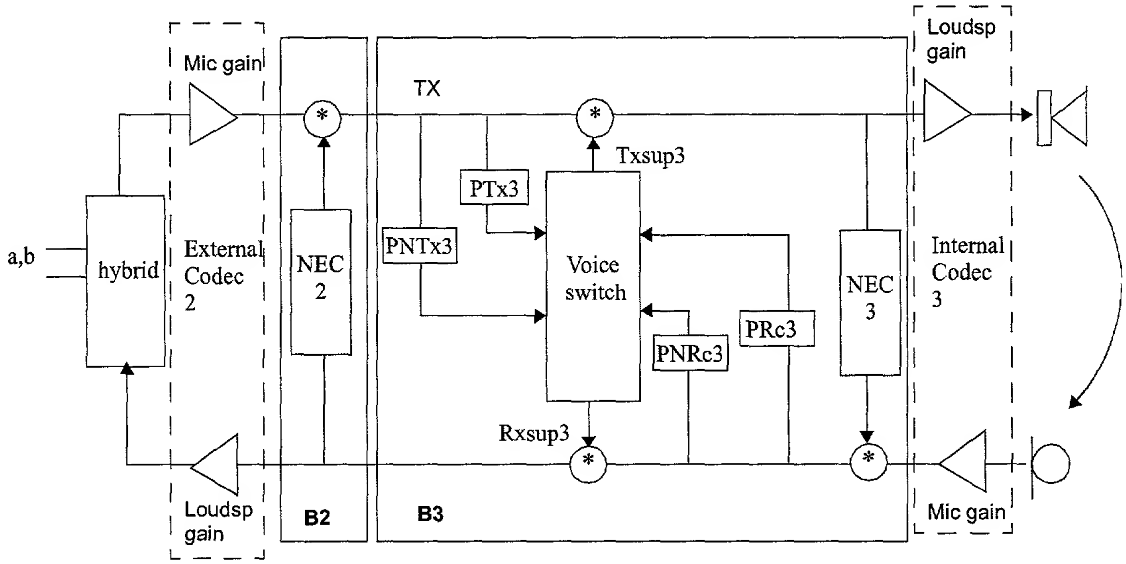


FIGURE 31. Handsfree functional diagram

The SC14424 speakerphone function has a full duplex quality behaviour using a combination of two near end *echo cancellers*, two echo suppressors with back ground level measurement. (see Figure 31)

The voice switch (VS) controls the switching priority between talker and listener.

The VS has the following **outputs**:

- **Txsup3**: The transmit signal suppression factor
- **Rxsup3**: The receive signal suppression factor

The VS **input** signals are:

- **PTx3**: *Transmit level power*
- **PNTx3**: Transmit noise level power
- **PRc3**: Receive level power
- **PNRc3**: Receive noise level power

The VS has three **region** switching characteristic as shown in Figure 32.

Transmit region

Txsup3 = LTxoff
Rcsup3 = LRcon

Receive region

Txsup3 = LTxon
Rcsup3 = LTxoff

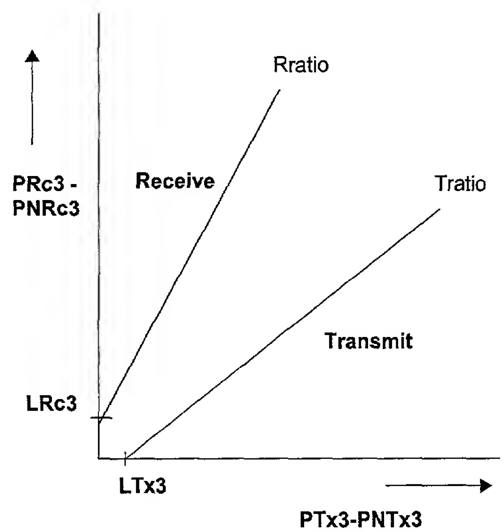


FIGURE 32. Voice switch characteristics

The regions are determined by a programmable **ratio** between transmit and receive level:

- **Rratio:** The Tx/Rc ratio to switch from Transmit to Receive state.
- **Tratio**: The Tx/Rc ratio to switch from Receive to Transmit state.

Listening-in

The listening-in function can be realised by adjusting the voice switch characteristic to an not sensitive level for the microphone. To prevent howling introduced by a cordless set, a Larssen level limiter can be realised by measuring the power of the transmitted signal in combination with a frequency measurement. This is done with the zero crossing detector ECZ1 or ECZ2 to measure the howling tone in the 300 to 3 kHz region.

4.7.16 ECP switch table

The function of the switch table is to connect outputs of DSP functional blocks to the and inputs of other blocks. The number of switching possibilities is reduced to limit the number of 125 usec delay for each copy cycle.

The switch table (see Table 9) is stored in RAM and must be programmed for each configuration of EDF_DSP.

As an example to connect the echo canceller block 2 to the Caller-id detector, the switch table entry 484 swcidin must be loaded with address 287 eh2out, so RAM[swcidin] = (ehs3out).

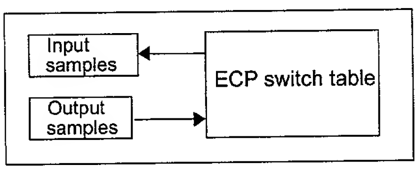


FIGURE 33. ECP switch table

Table 7: ECP switch table

Address (*2 + F200)	Input	Output pointer of block to connect to input swxxx
459	swhs1out	
460	swhs2out	
461	swehs1in	
462	swehs2in	
463	swehs3in	
464	swb1in	
465	swb2in	
466	swb3in	
467	swlinlaw1	
468	swlinlaw2	
469	swb1out	
470	swb2out	
471	swb3out	
472	swb2pcmout	
473	swlawlin2	
474	swchs1in	
475	swchs2in	
476	swcb1in	
477	swcb2in	
478	swsumin1	
479	swsumin2	
480	swsumin3	
481	swsumin4	
482	swagcin	
483	reserved	
484	swcidin	

Table 8: ECP output pointers

Address (*2 + F200)	Output pointer	Description
273	hs1in	ADPCM output
274	hs2in	ADPCM output
275	b1in	lin. input from line B1
276	b2in	lin. input from line B2 (external codec)
277	b3in	lin. input from line B3 (codec2)
278	b2pcmin	pcm input from line B2
279	b1out	output to line B1
280	b2out	output to line B2
281	b3out	output to line B3
282	b1lawlin	output pcm to lin conv.
283	b2lawlin	output pcm to lin conv.
284	b2linlaw	output lin to pcmconv.
285	ehs1out	output to ADPCM (after suppressor)
286	ehs2out	output to ADPCM (after suppressor)
287	ehs3out	output to ADPCM (after suppressor)
288	ec2out	output to ADPCM (before suppressor)
289	ec3out	output to ADPCM (before suppressor)
290	chs1out	Conference
291	chs2out	Conference
292	cb1out	Conference
293	cb2out	Conference
294	sumout1	output summator 1
295	sumout2	output summator 2
296	agcout	AGC output
297	reserved	
255	toneout	(DTMF) tonegenerator

4.8 LINE INTERFACE

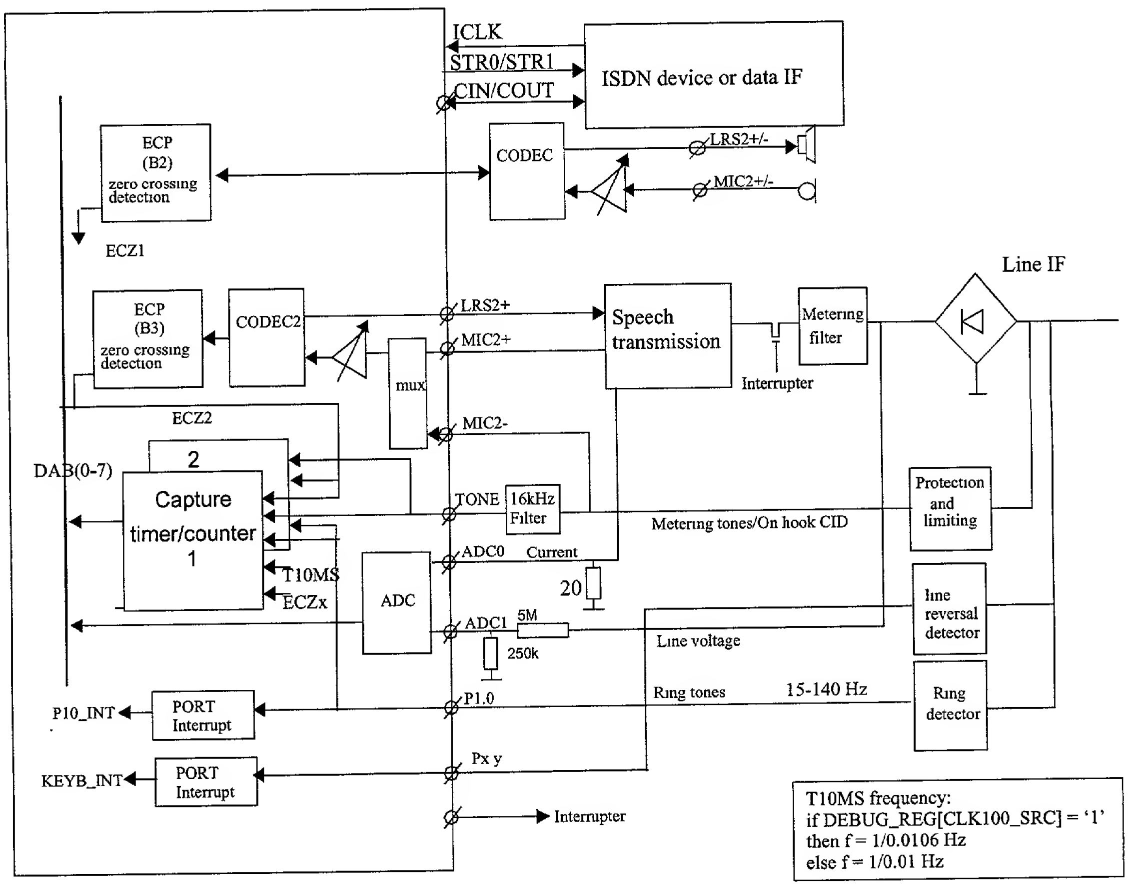


FIGURE 34. Complete line interface

4.8.1 On-chip codec interface

The SC14424 has one integrated Codec which can be either configured as a single ended input/output for connection to PSTN line interface circuits or as fully differential analog front end for connection to several types of microphones and loudspeakers (see Figure 36)

Line interfacing

The input configuration can be set with Codec_control_regB2[1,0]. (see Table 9) If M1, M0 = "10", the CAP2- is single ended input to receive Caller-id data, else if "01" the MIC2+ input is selected. To set output LRS2+ as a is the single ended output, Bit 6, SINen = '1' must be set. LRS- is not driven in this case.

Microphone/loudspeaker interfacing

Dynamic loudspeakers with an impedance as low as 100 Ω or ceramic loudspeakers with an equivalent resistance of 600 Ω and 100 nF capacitance can be connected to pins LRS2+/LRS2- without additional circuitry. The loudspeaker attenuation can be controlled from 0 to -15 dB in steps of 1 dB. For handsfree and listening-in application external an loudspeaker amplifier must be connected.

Several types of microphones can be connected to the MIC+/MIC- pins. The microphone gain is programmable from 0dB upto plus 30dB in steps of 2dB.

For active microphones a current source with high supply voltage rejection ratio is provided supply pins VREF+/ VREF-. PSTN line interface circuits can be connected differentially or single ended.

The microphone and loudspeaker gain of the on-chip codec can be adjusted to the required levels. The Codec_ control_registers can be loaded from the shared data RAM into the codec with the <C_LD2> command. The codec can be switched on/off with command <C_ON2>, <C_OFF2>.

Table 9: **codec 2 control registers**

Word	Bit7	Bit6	Bit5	Bit 4	Bits 3	Bits 2	Bits 1	Bits 0
B[0]	Off = $3D_{16}$, Stand-by FF_{16}, Active = $C2_{16}$							
B[1]	LIMen 0 = Limiter off 1 = Limiter on	SINen 0 = Differential 1 = Single ended LRS	-				M1, M0 00 = Normal Differential I/O 01 = Single ended MIC2+ 10 = SIngle ended CAP2- 11 = MIC2+/- disabled	
B[2]	LRSatt[3-0] in 1 dB steps				Micgain[**3-0**] in 2dB steps (if LIMen = 0)			
B[3]	Normal operation = C0							
B[4]	Normal operation = 00							
B[5]	Normal operation = 00							

4.8.2 Analog limiter

To prevent clipping of the receive signal in the digital domain an analog limiter can be enabled which B[1] bit7:LIMen. If this bit is 1 the initial codec gain can be programmed via the EDF_ECP. If the signal level reach CxLVL1 (x=1,2), the MICgain is reduced with steps of 2 dB. If the signal level goes below CxLVL2 (x=1,2), the MICgain is increased again until its initial value. The attack and decay times are programmable and levels are programmable for both codecs.

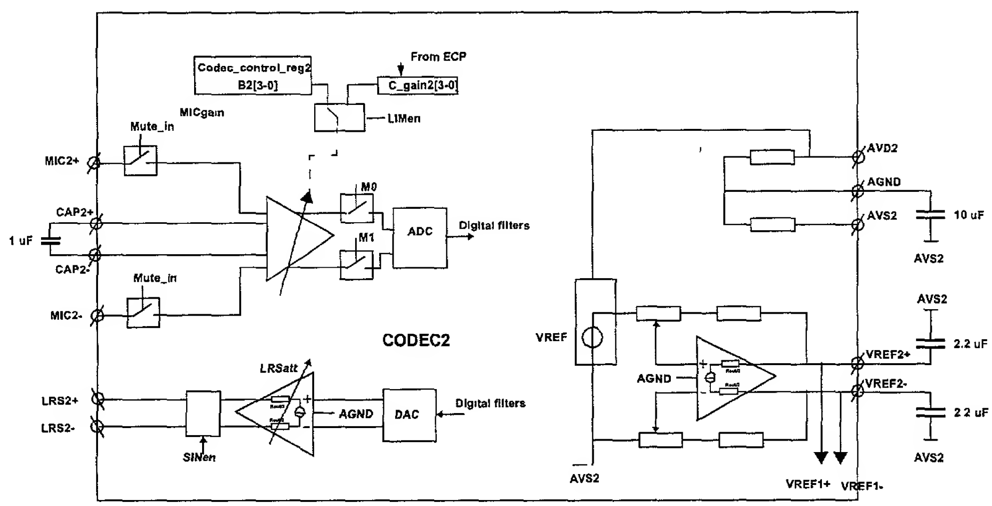
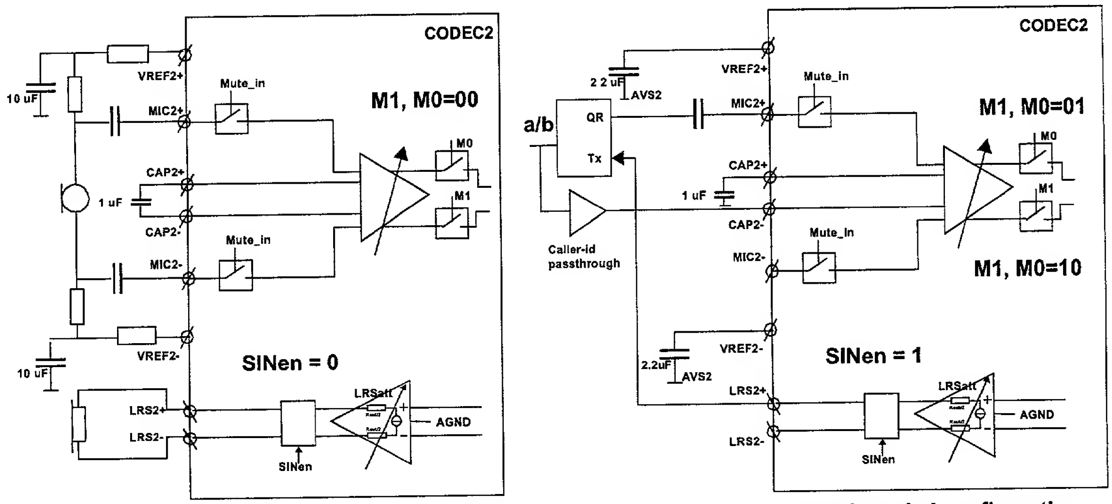


FIGURE 35. **Analog front end**



Differential configuration with microphone and earpiece

Single ended configuration for line interface

FIGURE 36. Analog front end configurations

4.8.3 Capture timer/counters

The SC14424 has a two programmable capture timer/ counters to measure frequencies of tones coming from the PSTN line. Figure 34 shows a complete line interface. The capture timer can either measure the time between two zero crossings (timer operation) or measure the number of zero crossing during a programmable time interval (counter operation).

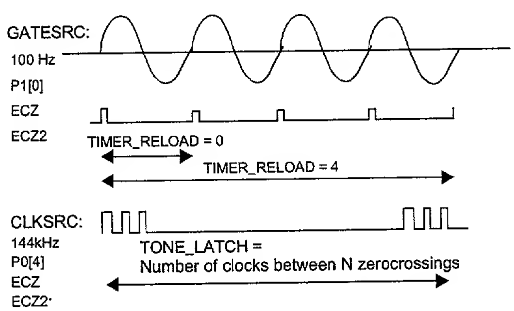


FIGURE 37. Timer/counter operation

The sources to measure the time between the zero crossings are selected with GATESRC. The clocks that count the number of cycles are selected with CLKSRC in counter TONE_COUNTER.

- GATESRC selection:
  - 00 = 100 Hz, the internal clock DECT frame clock
  - 01 = P1[0] for ring tone detection
  - 10 = ECZ, for call progress tone detection via MIC1 or CID measured behind the internal echo canceller 1
  - 11 = EZC2, for call progress tone detection via MIC+/- measured behind internal echo canceller 2.
- The CLKSRC selection:
  - 00 = 144 kHz, an internal clock
  - 01 = TONE input at P0[4] for metering tone detection.
  - 10 = ECZ, for tones from MIC1 or CID measured behind the internal echo canceller 1
  - 11 = EZC2, for tones from MIC+/- measured behind internal echo canceller 2.

The formula below shows the relation between the inputs:

TONE_LATCHx = (TIMER_RELOADx+1).*$F_{GATESRC}/F_{CLKSRC}$

The value of TONE_LATCH can be read out during interrupt routines:

- CLK100_INT if the 98Hz source is selected
- P1_0_INT if P1[0] is selected
- TIM0_INT or TIM1 if ECZx is selected

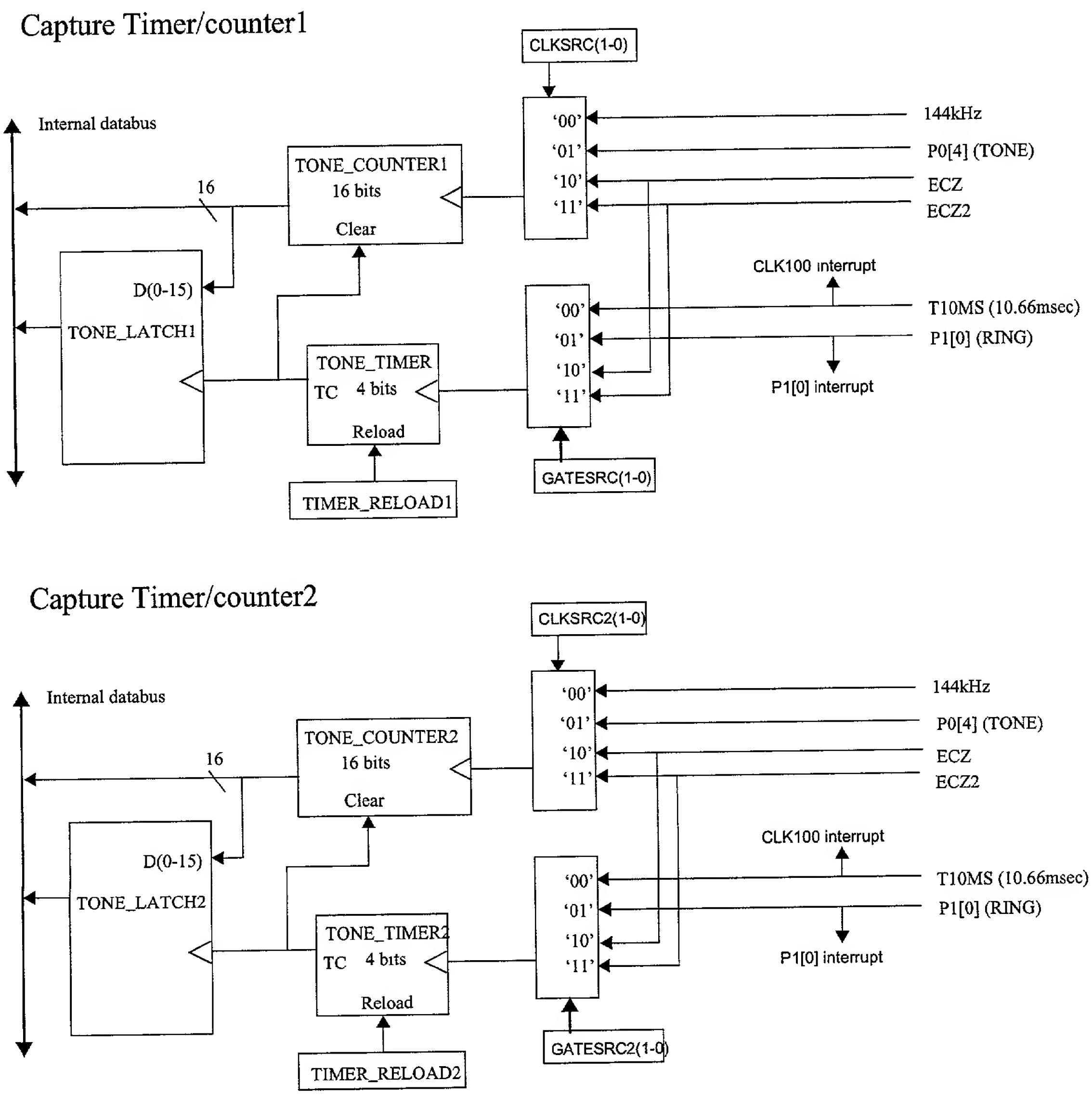


FIGURE 38. Capture timers block diagram

4.9 MAC FUNCTIONS

Receive and transmit burst timing on the RF interface is controlled by the DIP. All MAC-CSF functions are depicted in Figure 39. With DIP command <B_RC d_offset>, the control information can be read from any Data RAM location (see table 10). Control information is read before every received and transmitted slot. MAC status information on received slots is written into the data RAM of the SC14424 (see table 11). DIP command <B_WRS d_offset> updates all these parameters. At the end of every received time-slot an interrupt instruction <U_INTx> can be set in the sequencer RAM to enable the microprocessor to read out the appropriate status data.

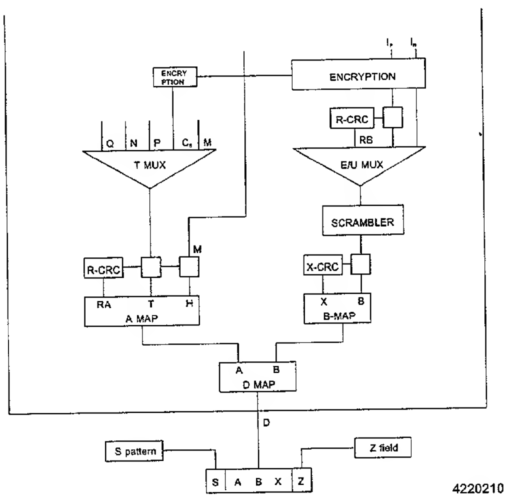


FIGURE 39. SC14424 MAC functionality

Table 10: MAC control information in Data RAM

NAME	TYPE	FUNCTION
S_err[3..0]	Binary	Maximum number of errors allowed in non-masked bits of S-field pattern S[8..31]
Inv_RDI		Inversion of received data input
Inv_TDO		Inversion of transmit data output
SENSE_A		B field data is not written in the case when the A-field CRC is incorrect
PP/FPn		PP mode selected
Mask[3..0]	Binary	Mask S-field pattern[15..8] in error calculation over pattern [8-31]
Slide[3..0]	Binary	Mask S-field pattern[15..8] in Sliding error calculation over pattern[15-8]
DAC[5..0]	Binary	DAC output value to control DAC pin 27

Table 10: MAC control information in Data RAM

NAME	TYPE	FUNCTION
ADP		Upon A-field CRC error, no phase adjustment will be made
WIN[3..0]	Binary	Defines maximum phase shift. If phase shift is between ±WIN symbols, the IN_SYNC bit will be set
VOL[5..0]	Binary	TDO gaussian output volume control. Default '100' mid value after reset.
M[1..0]	Code	TDO output mode: 00 = digital output 01 = Gaussian output 10 = power down 11 = mid level
FR_nr[3..0]	Binary	Frame number 0..15
MFR[23..0]	Binary	Multi frame number
IV[28..63]	Code	Encryption unit initialisation vector
CK[0..63]	Code	Encryption unit cypher key
ENC_ON	Code	Enable/disable Encryption

4.9.1 Slot synchronisation

The SC14424 is capable of detecting the S-field pattern. To be able to lock to the received frame in the PP mode the microprocessor enables the slot counter to be preset at S-field detection. If the preset of the slot counter occurred once, the preset is disabled. The microprocessor can enable this preset again. If disabled the SC14424 will only search for the S-field pattern in a predefined window repeated every 10ms after the first S-field pattern has been detected. In lock the SC14424 can accept a packet phase shift up to a programmed maximum window size. This window is programmable with control nibble WIN[3:0] from 0-15 symbol periods. This phase shift information is stored in PHASE[7:0] in two's complement notation in the MAC status bytes. If the phase shift is more than the programmed window the "in_sync" bit will be reset. Once enabled by the microprocessor the SC14424 will automatically adjust the frame timing. If the ADP bit is set '1' then the automatic phase adjustment will only be done if the A-field CRC is correct. If ADP is '0' the phase adjustment will be made regardless of the A-field result. Choosing to write the B-field data depending on the A-field CRC result is selectable using the control bit SENSE_A. If the phase shift between the internally generated frame and received frame is less than 2 symbol periods frame timing is adjusted with ±1 symbol period at the end of the frame. The update will be maximum ±2 symbols if the phase shift is 2 or more symbols. However the microprocessor can take over control and program phase jumps of ±1 symbol period instructions for the next frame if appropriate and disable the automatic phase jumps.

The microprocessor programs a jump instruction to the right slot address in the timing RAM once the Qt message is received and decoded and thus presets the slot-counter.

If the BMC looses synchronisation and the SenseS flag is set, no B field will be written and the In_sync bit will be set to '0'.

4.9.2 S-pattern correlator

With the control bytes it is possible to define the criteria for the S-field to be detected.

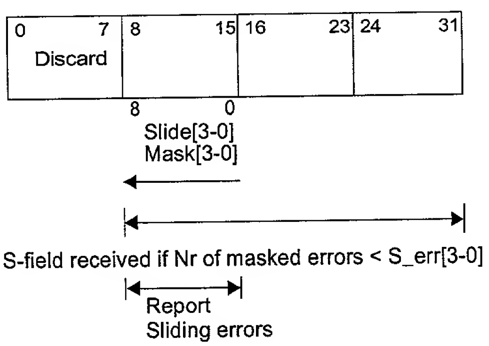


FIGURE 40. S-field pattern

The first eight bits of the S-field [7-0] bit sync pattern are ignored. On the next eight bits a mask register Mask[3-0] masks bits 15 to 8. ("0011" unmasks bit 13,14,15.). If the total number of errors in bits 16 to 31 plus the unmasked bits 8 to 15 is less than a number programmed in the data RAM (S_err[3-0]), the S-field is received correctly and the phase shift can be calculated. S-field bits 15 through 8 are also used to check for sliding errors. These are reported in the MAC unit status register SL_err[3:0]. Mask register Slide[3-0] masks S-field bits 15-8. ("0011" unmasks bits 13,14,15). Only unmasked bits are taken in to account for the sliding error calculation. A sliding error occurs when a neighbouring un-synchronized station sends out a packet that slides into the received packet.

4.9.3 Encryption

The Key Stream Generator (KSG), used to encrypt A and B-field information, can be switched on or off by the microcontroller via instructions in the sequencer RAM. The KSG initial state is stored in the internal data memory. CK[63:0] is the cypher key information. The MAC unit recognizes Cs type messages in the A-field data and encrypts or decrypts only these messages.
Encryption can be enabled or disabled with bit ENC_ON.

4.9.4 Scrambler

Scrambling and descrambling, using the frame counter bits FR_nr[2:0] to initialize the scrambler and de-scrambler, is performed on the B-field.

4.9.5 R-CRC, X-CRC and Z field

Generation and checking of the 16-bit CRC is performed on the A-field data (A_CRC will be set if CRC is correct). For the B-field, X-CRC and Z-field are generated and checked for transmission and reception respectively. A, X and Z field results are stored in the internal data memory (A_CRC, X_CRC and ZACK bit). Full and double slot protected B-field format is supported and 16 bit CRC is calculated for every 64 bits of data.

4.9.6 Data storage

At the end of every received slot the status is updated in the Data Memory.

A-field data and B-field data are fetched and stored in the internal data memory. The user can define as many memory locations and subbanks for different slots and / or A-field messages as needed.

Table 11: MAC status information in Data RAM

NAME	TYPE	FUNCTION
ADC[5-0]	Binary	Maximum RSSI peak value measured during PD0.
IN_SYNC		Set to '1' when the S-Field pattern falls within the defined window size
A_CRC		Set to '1' when the A-field CRC is correct
X_CRC		Set to '1' when the X-field CRC is correct
ZACK		Set to '1' when the Z-field = X-field
Bn-CRC		Set to '1' when protected B field R-CRC of block n is correctly received. n =1-10
SL_err[3-0]	Binary	Report number of sliding errors over unmasked S-field bits 8 to 15.
TAP[4-0]		S-field phase information
Phase[7-0]	2's Compl	S-field pattern phase error
DC[5-0]	Binary	DC offset information

4.10 CompactRISC^{TM} Peripherals

4.10.1 Digital to Analog convertors (DAC)

The SC14424 has an two identical 8-bit Digital Analog Converter (DAC). The DAC output pin supplies the voltage set in register DAC_REG. After a reset, register DAC_REG is set to 80_{16} and the DAC conversion is started if AD_CTRL_REG.DAC_PD = '0'. This setting results in a "mid-level" voltage (= (AVD-AVS) * (125/255)) at the DAC pin directly after reset. After reset the output voltage can be changed continuously through register DAC_REG. If the AD_CTRL_REG.DAC_PD = '1', the DAC is switched off and the output pin is connected to AVD.

4.10.2 Analog to Digital convertor (ADC)

The SC14424 has a three input successive approximation 8-bits ADC. The ADC gives full scale (255) if the voltage on ADC0,1,2 is AVD. The Vin input range is:

AVD*(ADCval/255) < Vin < AVD*(ADCval+1)/255.

To measure higher voltages, a resistor divider should be applied externally. The maximum source resistance is 350kohm. The ADC is enabled after the DIP command <C_LD>. The A/D conversion is started if ADC_START is set to '1'. After conversion this bit is cleared. The inputs can be selected with AD_SEL[3-2] bits in the AD_CTRL_REG (see Table 52). If value '11' is selected, ADC-DAC is switched to ADC0 pin. The ADC-DAC value can be set by writing to ADC_REG.

4.10.3 Input/Output Ports 0,1,2

The SC14424 has 21 programmable I/O pins (Port 0, 1, 2) These pins are used as general I/O pins or as internal peripherals I/O. Each I/O pin has a direction and data input/ output bit. For easy programming port 0 and 1 have a set and reset data register. In this way bit masking is not needed

4.10.4 Port 0 UART

The SC14424 has a full duplex UART with 1 start bit, 8 data bits, 1 stop bit and no parity. The UART clock is derived from the 1.152MHz or 10.368 MHz DECT clocks divide by 10,20,60 or 120. The UART baud rate is programmable to 115.2 kBaud, 57.6 kBaud, 19200 or 9600 Baud in case the 1.152 MHz is selected or 1036.8, 518.4,172.8, 86.4 KHz in case of10.368 MHz. The receiver accepts s a clock jitter of 2%. Data loaded in the UART transmit register P0_UART_TX_REG is transmitted on pin P0.0/TX. The register is **only** reloaded if the start bit, 8 data bits and stop bit are transmitted and the TI bit is 0 (no UART interrupt pending). After the FIFO is reloaded the UART interrupt pending bit is set to 1. The RI/TI interrupt source can be read in P0_UART_CTRL_REG bit 2 and 3. In order to use the RI and TI on same interrupt, the interrupt UART_INT_PEND bit must be cleared in the interrupt service routine. This allow the second UART interrupt to be handled as a nested subroutine.

Data received on pin P0[1]/RX is copied in P0_UART_RX_REG after reception of the stop bit. After transferring the data to the P0_UART_RX_REG the UART interrupt pending bit is set to 1. After (10 * Rx/Tx Clock) the data received in the P0_UART_RX_REG is overwritten by the next received data bit.

Note: P0_UART_RX_REG and P0_UART_TX-REG are two registers mapped on the same address.

After system reset the P0[0] is floating and P0[1] is connected to a pull down resistor. This way the UART receive and transmit can be combined to a one wire UART.

4.10.5 Port 0 Environment register

On the rising edge of RSTN, port 0 is latched in the register ENV_P0_ENV_REG. The value of the environment register together with TP=1 (pin #50) determines the start-up of the boot program and selects test modes. See table 31 page 53 for a detailed description of the environment register.

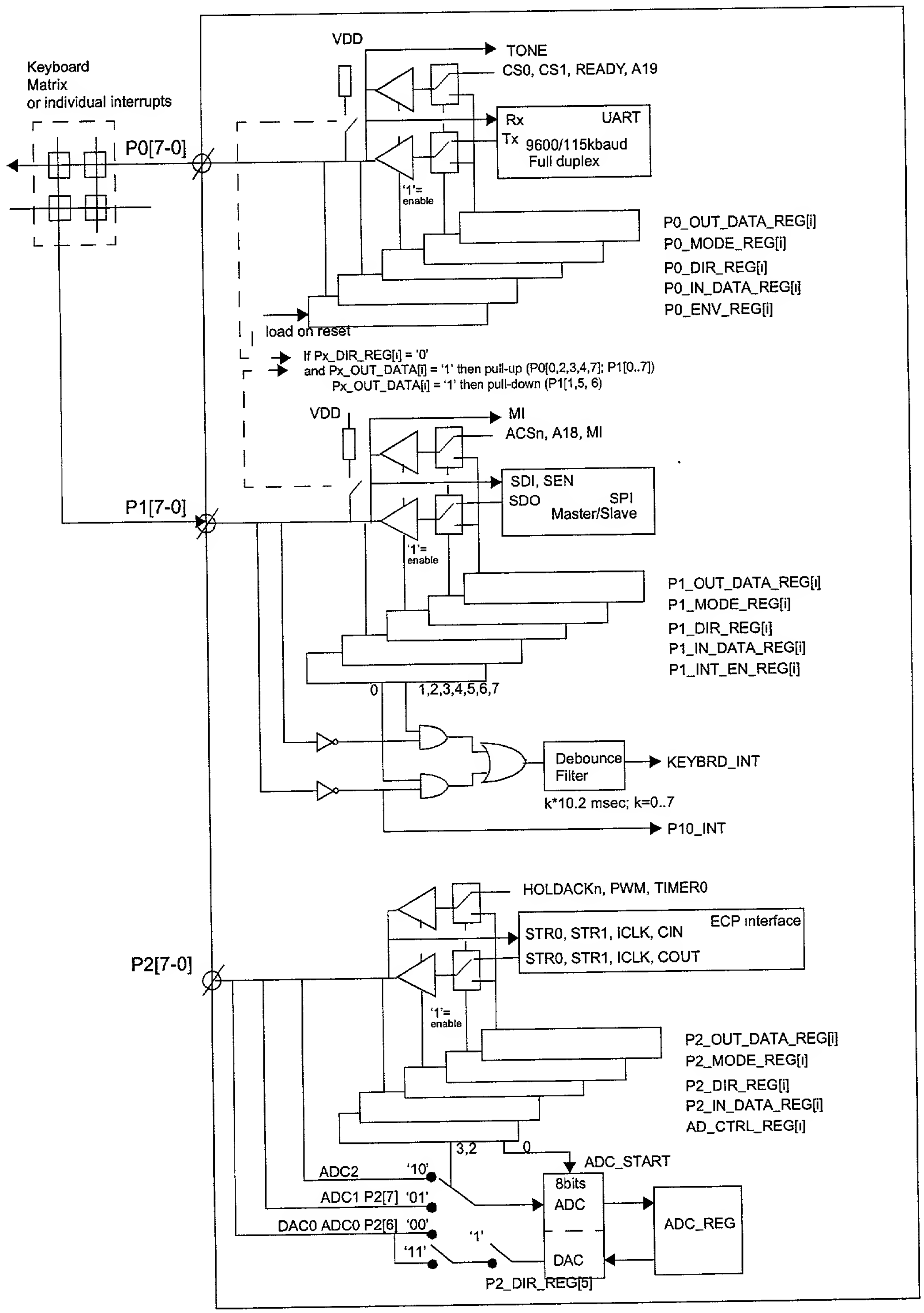


FIGURE 41. Port 0,1,2 configuration

4.10.6 Port 1 SPI

The SC1424 has a serial synchronous interface to supports SPI™*. The serial interface can transmit and receive n*8bits in master and slave mode

The interface signals are:

- SDI: Serial data input
- SDO: Serial data output.
- SCK: Serial data clock. Master or slave
- SEN: Serial enable slave only.

The SCK signal polarity and active clock edges can be selected as shown in Table 12. The SCK phase can be set with bit SPHA and the idle level polarity with bit SPOL in the SPI_CTRL_REG. (Table 45 on page 57)

Master mode can be selected with SPI_CTRL_REG[SPI-MODE] = '1'. In master mode SCK can be set to four clock frequencies 36 kHz, 72 kHz, 144 kHz and 576 kHz and SEN can be any of the SC14424 I/O ports and must be set by the CR16. This allows a multi-slave operation. If slave, bit SPI_MODE must be '1' and SEN must be set to input signal with P1_DIR_REG[2] is '0'. If switching between master and slave mode, SEN must be '0'. Figure 42 shows the timing diagram in master and slave modes.

If slave mode is selected, data for SPI can be loaded in the SPI transmit register P1_SPI_RX_TX_REG and will be transmitted on pin P1[4]/SDO. Simultaneously the register P1_SPI_RX_TX_REG is loaded with data received on P1[3]/SDI.
After 8 clock cycles bit SPI_INT_PEND is set. This bit can be read in registers SET_INT_PEND_REG and RESET_INT_PEND_REG. If SPI_INT_PEND is set and SPI_INT_REG has a value unequal to 0, a maskable interrupt to the CR16B will be generated. (See also chapter 4.2.6. ICU.) The interrupt must be cleared by writing a '1' to RESET_INT_PEND_REG bit SPI_INT_PEND.

Table 12: SCK clock modes and active edges

SPHA	SPOL	SCK idle level	SDO	SDI
0	0	Low	↓	↑
0	1	High	↑	↓
1	0	Low	↑	↓
1	1	High	↓	↑

* SPI™ is a trademark of Motorola

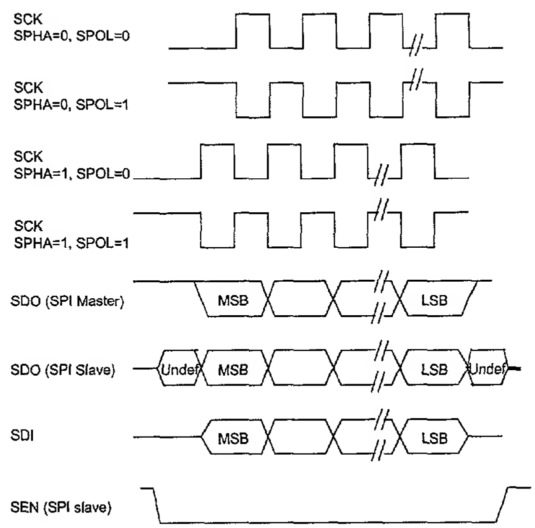


FIGURE 42. SPI timing diagram

4.10.7 Port 1 Interrupts

The SC14424 port 1 can be programmed to generate interrupts from one or more port pins. P1[0] can generate an individual interrupt P10_INT while P1[0,1,2,3,4,5,6,7] can generate a KEYBRD_INT if one of them goes low (Figure 41).

Together with port 0 a keyboard can be made. No external components are needed except for the key switches. The keyboard matrix has a maximum size of 8 columns and 8 rows. To off-load the CR16B a programmable debounce filter is integrated. Every keyboard row is attached to a P1 pin. By writing a 1 to the P[x] output data register and a 0 to the P1[x] direction register a pull-up resistor is connected. The data input is connected to the keyboard debounce filter after the P1[x] interrupt register is set to 1. The keyboard columns are attached to P0. Every column is connected to a P0 pin. The P0[x] pins are configured as output, P0[x] Direction register is 1 and the P0[x] data output is set to 0. If a keyboard switch is pressed the P1[x] pin becomes 0 and the debounce filter is triggered. Only the keyboard switch is still pressed after the debounce time a keyboard interrupt is generated. After the application keyboard interrupt service routine is called the keyboard scanning starts.

If P1 pins are used for other functions which require an interrupt, the interrupt service routine of these functions must be combined with the keyboard scan interrupt service routine.

4.10.8 Port 2 Timers 0 and 1

The SC14424 has two general 16 bits purpose timers TIMER0 and TIMER1. Each of the timers is represented by 2 16-bit registers. The timer input clock for TIMER1 is fixed to 1.152 MHz. The clock for TIMER0 is selectable between 1.152 and 10.368 MHz with CLK_SEL in the TIMER_CTRL_REG. Both timers can operate in Timer mode or PWM mode.

Timer Mode

The timer M and N reload registers determine the timer cycle and width 'H' time. If TIMER_CTRL_REG bit 0 or 1 is set to 1 the timer is started. At that moment the M reload value is loaded the 16 bit counter starts to count downwards. The 16 bit counter is decremented at a clock rate of 1.152 MHz or 10.368 MHz (timer0 only). If the counter reaches 0 the following actions are performed:

- reload value N is loaded into the 16 bit counter.
- the timer interrupt pending bit is set to 1.

The N reload value is also decremented with a rate of 1.152MHz. If the counter reaches 0 again the following action is performed:

- reload value M is loaded into the 16 bit counter.

This process of reloading the M and N registers is repeated until the timer is stopped by setting the timer control bit 0 or 1 to 0. The reload values M and N can be updated at all times regardless if the timer is running.

The actual value of both counters can be read

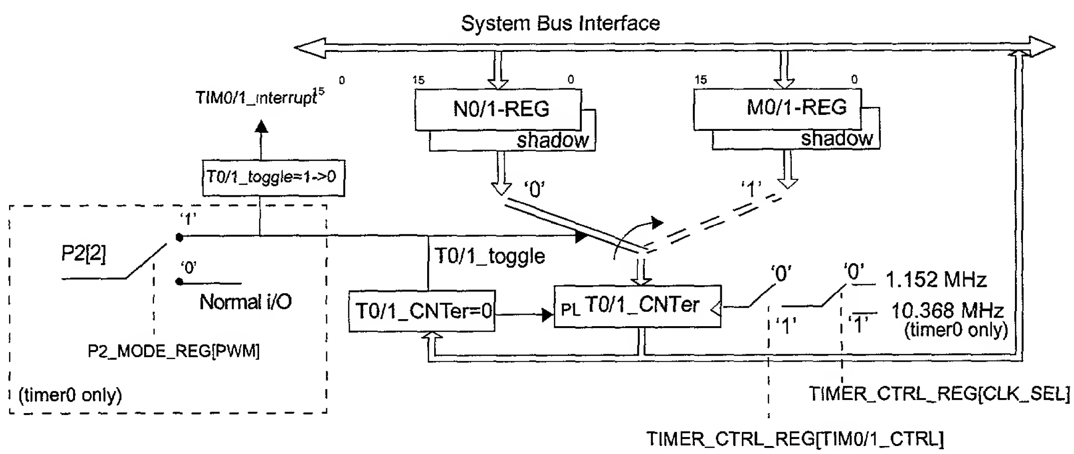


FIGURE 43. Timer 0 and 1

PWM Mode

In PWM mode the envelop of timer 0 is output to port P2[PWM]. The PWM mode is enabled with P2_MODE_REG[PWM] set to '1' while P2_DIR_REG[2] is set to input.

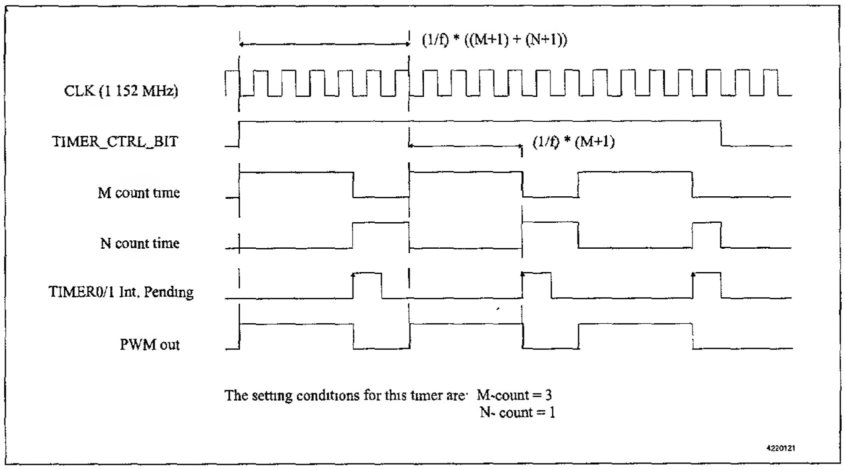


FIGURE 44. Timer 0 and 1 Timing

4.10.9 Watchdog Timer

The watchdog timer is a 8-bit timer that can be used to detect an unexpected execution sequence caused by a software run-away.

The watchdog timer consists of 8 bits, its contents is decremented by 1 every 10msec. The WATCHDOG_REG is set to FF_{16} at reset. This results in the maximum watchdog time of 2.56 seconds. If the watchdog reaches 0 a non maskable interrupt is generated and the WATCHDOG_REG is set to FF_{16} again.

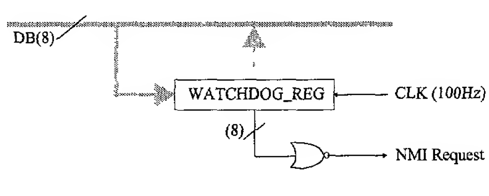


FIGURE 45. Watchdog timer

4.10.10 Clock 100 Timer

If CLK100_SRC bit in the DEBUG_REG is '0' then the clock 100 timer has a time period of 10 msec, synchronised to the execution of a DIP timer. If CLK100_SRC is '1' the clock 100 is a continuous signal with a time period of 10.6 msec. The clock 100 timer (10msec) is started if the sequencer program is started (URST = "0"). The clock 100 timer rising edge is synchronised to the DIP SLOT_ZERO command. The clock 100 interrupt pending bit is set on every rising edge of clock 100. When the sequencer program is stopped (URST = "1") the clock timer is also stopped

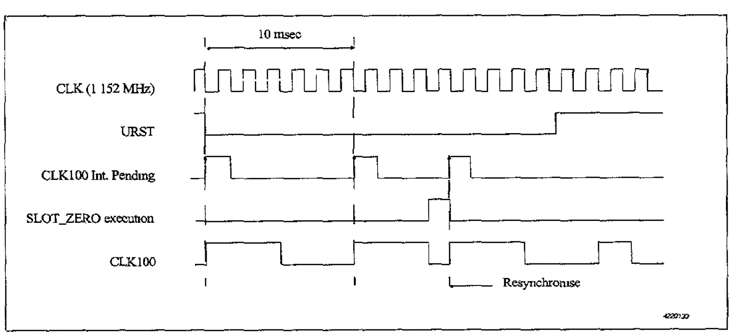


FIGURE 46. Clock 100 Timing

4.11 ON-CHIP REGISTERS (OVERVIEW)

Table 13: Memory Map of internal Register

Address	Port	Description
F200$_{16}$ F5FB$_{16}$	ECP control registers	ECP Parameters, Switching table, etc.
F5FC$_{16}$	FSK_DATA	FSK received data
F5FD$_{16}$	ECP_MASK_REG	TONE_INT, FSK_INT mask register.
F5FE$_{16}$	ECP_STATUS_REG	TONE_INT, FSK_INT status. Cleared if read
F5FF$_{16}$	PHASE INFO	Difference between rising edge of internal and STR0 8 kHz in units of 434 nsec.
F600$_{16}$ F9FF$_{16}$	Reserved	
FA00$_{16}$ FBFF$_{16}$	Sequencer RAM	
FC00$_{16}$ FEFF$_{16}$	CR16 internal interrupt vectors	
FF02$_{16}$	RESET_INT_PENDING_REG1	Clear interrupt, reading returns interrupt status
FF03$_{16}$	RESET_INT_PENDING_REG2	Clear interrupt, reading returns interrupt status
FF04$_{16}$	SET_INT_PENDING_REG1	Generate interrupt, reading returns interrupt status
FF05$_{16}$	SET_INT_PENDING_REG2	Generate interrupt, reading returns interrupt status
FF06$_{16}$	INT_REG1	Set priority level: KEYB_INT and P10_INT (0=lowest, 7=highest)
FF07$_{16}$	INT_REG2	Set priority level: UART_INT and SPI_INT (0= lowest, 7= highest)
FF08$_{16}$	INT_REG3	Set priority level: TIMER0_INT and TIMER1_INT (0=lowest, 7=highest)
FF09$_{16}$	INT_REG4	Set priority level: CLK100_INT and DIP (0=lowest, 7=highest)
FF0A$_{16}$	INT_REG5	Set priority level:CLK8K_INT and TONE_INT (0= lowest, 7= highest)
FF10$_{16}$	P0_IN_OUT_DATA_REG	P0 Data register
FF11$_{16}$	P0_SET_OUTPUT_DATA_REG	P0 set port pins register
FF12$_{16}$	P0_RESET_OUTPUT_DATA_REG	P0 reset port pins register
FF13$_{16}$	P0_DIR_REG	P0 direction register
FF14$_{16}$	P0_MODE_REG	Select CS0,1,2, AD18, AD19, CLK100
FF15$_{16}$	P0_CSMODE_REG	Select CS0,1,2 modes
FF16$_{16}$	P0_ENV_REG	CR16B boot mode control register
FF17$_{16}$	P0_TEST_CTRL_REG1	Test control register 1
FF18$_{16}$	P0_TEST_CTRL_REG2	Test control register 2
FF19$_{16}$	P0_UART_CTRL_REG	UART control register
FF1A$_{16}$	P0_UART_RX_TX_REG	UART data transmit/receive register
FF1B$_{16}$	P0_UART_CLEAR_TX_INT	UART clear transmit interrupt
FF1C$_{16}$	P0_UART_CLEAR_RX_INT	UART clear receive interrupt

Table 13: Memory Map of internal Register (Continued)

Address	Port	Description
FF20$_{16}$	P1_IN_OUT_DATA_REG	P1 Data register
FF21$_{16}$	P1_SET_OUTPUT_DATA_REG	P1 set port pins register
FF22$_{16}$	P1_RESET_OUTPUT_DATA_REG	P1 reset port pins register
FF23$_{16}$	P1_DIR_REG	P1 direction register
FF24$_{16}$	P1_MODE_REG	Enable SPI and p1[0] interrupt level
FF25$_{16}$	P1_INT_EN_REG	P1 keyboard interrupt enable register
FF26$_{16}$	P1_DEBOUNCE_REG	P1 keyboard debounce timer register
FF27$_{16}$	P1_SPI_CTRL_REG	SPI control register
FF28$_{16}$	P1_SPI_RX_TX_REG	SPI data transmit/receive register
FF30$_{16}$	P2_IN_OUT_DATA_REG	P2 Data register
FF31$_{16}$	P2_SET_OUTPUT_DATA_REG	P2 set port pins register
FF32$_{16}$	P2_RESET_OUTPUT_DATA_REG	P2 reset port pins register
FF33$_{16}$	P2_DIR_REG	P2 direction register
FF34$_{16}$	P2_MODE_REG	P2 I/O selection.
FF40$_{16}$	AD_CTRL_REG	P2 DAC, ADC start, ADC selection
FF41$_{16}$	ADC_REG	8 bits ADC value or 8 bits DAC if ADC disabled
FF42$_{16}$	DAC_REG	8 bits DAC value
FF43$_{16}$	DAC2_REG	8 bits DAC value
FF44$_{16}$	TONE_MUX_REG	Timer reload value, Timer clock mux select, Counter source select, Tone source select.
FF45$_{16}$	TONE_MUX_REG2	Timer reload value, Timer clock mux select, Counter source select, Tone source select.
FF46$_{16}$ FF47$_{16}$	TONE_ COUNTER_1L, TONE_COUNTER_1H	16 bits TONE_COUNTER_1 value which is latched periodically. TONE_COUNTER_H is MSB, TONE_ COUNTER_L is LSB.
FF48$_{16}$ FF49$_{16}$	TONE_ LATCH_1L, TONE_LATCH_1H	Contains the latched TONE_COUNTER_1 value TONE_LATCH_H is MSB, TONE_LATCH_L is LSB.
FF4A$_{16}$ FF4B$_{16}$	TONE_ COUNTER_2L, TONE_COUNTER_2H	16 bits TONE_COUNTER_2 value which is latched periodically. TONE_COUNTER_H is MSB, TONE_ COUNTER_L is LSB.
FF4C$_{16}$ FF4D$_{16}$	TONE_ LATCH_2L, TONE_LATCH_2H	Contains the latched TONE_COUNTER_2 value TONE_LATCH_H is MSB, TONE_LATCH_L is LSB.
FF52$_{16}$ FF53$_{16}$	TIMER0_RELOAD_M_REG	2 x 16 bits reload value timer for timer or PWM. M is counted down with 1.152 MHz. If zero an interrupt is generated and N is reloaded. If N becomes zero, M is reloaded. If M becomes zero N is reloaded. If selected as PWM timer, M is connected to PWM output P2[0] and represents the high time of the PWN signal and N the low time.
FF54$_{16}$ FF55$_{16}$	TIMER0_RELOAD_N_REG	
FF56$_{16}$ FF57$_{16}$	TIMER1_RELOAD_M_REG	2 x 16 bits reload value timer for timer or PWM. M is counted down with 1.152 MHz. If zero an interrupt is generated and N is reloaded. If N becomes zero, M is reloaded. If M becomes zero N is reloaded.
FF58$_{16}$ FF59$_{16}$	TIMER1_RELOAD_N_REG	
FF5A$_{16}$	TIMER_CTRL_REG	Starts timer 0 or timer 1.

Table 13: **Memory Map of internal Register** (Continued)

Address	Port	Description
$FF60_{16}$	CLK_DIV_REG	Bits 2-0 determines main clock divider 1,2,3,4,5,6,7,8 (default = 8)
$FF62_{16}$	AUX_CS_LOW_REG	Lower address boundary for auxiliary chip select (ACSn)
$FF63_{16}$	AUX_CS_HIGH_REG	Upper address boundary for auxiliary chip select (ACSn)
$FF64_{16}$	AUX_WAIT_REG	Number of wait states during auxiliary chip select (ACSn). Bits 2-0 select 0 to 7 wait states
$FF65_{16}$	SET_FREEZE_REG	Freeze watchdog, timer 1, timer 0 and DIP during debugging
$FF66_{16}$	RESET_FREEZE_REG	Release watchdog, timer 1, timer 0 and DIP during debugging after setting in freeze mode
$FF67_{16}$	DEBUG_REG	Set SC14424 debug modes.
$FF68_{16}$	WATCHDOG_REG	Watchdog preset value. Decremented every 10 msec. Generates NMI
$FF70_{16}$ $FF7F_{16}$	CS0_IO_REG	CS0 Data I/O register
$FF80_{16}$ $FF8F_{16}$	CS1_IO_REG	CS1 Data I/O register
$FF90_{16}$ $FF9F_{16}$	CS2_IO_REG	CS2 Data I/O register
$FFE0_{16}$	DIP_STACK_REG	DIP Stack pointer. (read only). The DIP stack is 4 deep
$FFE1_{16}$	DIP_PC	DIP program counter
$FFE2_{16}$	DIP_CTRL_REG	DIP Control register, clears DIP_INT if read
$FFE3_{16}$	DIP_STATUS	DIP Control register, returns DIP_CTRL_REG but does not clear DIP_INT
$FFF0_{16}$ $FFFE_{16}$	Reserved	Reserved for emulation
$FFFF_{16}$	VERSION	Contains ASCII value of SC14424 version.This value corresponds to the version number in the order number: SC14424VJG and SC14424RVJG is 'A', SC14424BVJG and SC14424BRVJG is 'B' etc.

4.12 ON-CHIP REGISTERS (DETAILED)

Table 14: ECP_MASK_REG(0.F5.FD)

BIT	MODE	SYMBOL	DESCRIPTION	RESET
7				
6	R	M_FSK_INT	Mask FSK_INT interrupt. '0' is disable, '1' is enable interrupt.	0
5	R	M_DTMF_INT_P	Mask DTMF_INT_P interrupt. '0' is disable, '1' is enable interrupt.	0
4	R	M_CAS_INT_P	Mask CAS_INT_P interrupt. '0' is disable, '1' is enable interrupt.	0
3	R	M_ST_INT_P	Mask ST_INT_P interrupt. '0' is disable, '1' is enable interrupt.	0
2	R	M_DTMF_INT_N	Mask DTMF_INT_N interrupt. '0' is disable, '1' is enable interrupt.	0
1	R	M_CAS_INT_N	Mask CAS_INT_N interrupt. '0' is disable, '1' is enable interrupt.	0
0	R	M_ST_INT_N	Mask ST_INT_N interrupt. '0' is disable, '1' is enable interrupt.	0

Table 15: ECP_STATUS_REG(0.F5.FE)

BIT	MODE	SYMBOL	DESCRIPTION	RESET
6	R/W	FSK_INT	Set if a FSK byte is received. A '0' to '1' transition sets TONE_INT. Cleared by writing a '0'.	0
5	R/W	DTMF_INT_P	Set if a DTMF tone is detected. The value can be read in the ECP_TONE_REG A '0' to '1' transition sets TONE_INT. Cleared by writing a '0'.	0
4	R/W	CAS_INT_P	Set if a CAS tone is detected. The value can be read in the ECP_TONE_REG. A '0' to '1' transition sets TONE_INT. Cleared by writing a '0'.	0
3	R/W	ST_INT_P	Set if a single tone is detected. A '0' to '1' transition sets TONE_INT. Cleared by writing a '0'.	0
2	R/W	DTMF_INT_N	Set if a DTMF tone detection has stopped. A '1' to '0' transition sets TONE_INT. Cleared by writing a '0'.	0
1	R/W	CAS_INT_N	Set if a CAS tone detection has stopped. A '1' to '0' transition sets TONE_INT. Cleared by writing a '0'.	0
0	R/W	ST_INT_N	Set if a single tone detection has stopped. A '1' to '0' transition sets TONE_INT. Cleared by writing a '0'.	0

Table 16: ECP _CONTROL_REG address 0 (MSB)

	15	14	13	12	11	10	9	8
	B2Sfir1	B2Sfir2	B2Srcv1	B2Srcv2	B2Srcv3	B2Srcv4		
	00 = disable 01 = 0dB 10 = 6dB 11 =12dB		00 = 0dB 01 = -6dB 10 = -12dB 11 = -18 dB		00 = switch off 01 = 0 dB 10 = 6 dB 11 = 12 dB			

Table 17: ECP _CONTROL_REG address 0 (LSB)

	7	6	5	4	3	2	1	0
	B3Sfir1	B3Sfir2	B3Srcv1	B3Srcv2	B3Srcv3	B3Srcv4		
	00 = disable 01 = 0dB 10 = 6dB 11 =12dB		00 = 0dB 01 = -6dB 10 = -12dB 11 = -18 dB		00 = switch off 01 = 0 dB 10 = 6 dB 11 = 12 dB			

Bit 7,6,5,4: Echo path gain

With B2Srcv1,2 and B3Srcv1,2 determine an attenuation of 0/-6/-12/-18 dB before the echo canceller. B2Srcv3,4 and B3Srcv3,4 determine an gain of 0/6dB/12 dB after the echo canceller. These bits can be used to increase the dynamic range of the echo canceller with 6 dB/12 dB.

Bits 3,2: Echo canceller error gain

With bits B2sfir1,2 and B3sfir1,2 the replica of the echo can be multiplied with 0,1,2 or 4. This is also done to increase the dynamic range of the echo canceller.

Table 18: ECP _CONTROL_REG address 1 (MSB)

value	15	14	9	13	12	11	10	8
	lawb1	lawb2	ECON	B2Stx1	B3Stx1	SAGC	FSKen	
0	A-Law	A-Law	B2 PCM coder active	0 dB	0dB	6dB	CAS/DTMF detectors enabled	
1	μ-Law	μ-Law	B2 EC active	6dB	6dB	12dB	FSK detector enable	

Bits 15,14: PCM coding

For external devices the PCM can be A-law or μ-law coded (for B1 and B2).

Bits 13,12 B2Stx

These bit determine the gain the transmit path after the limiter, before the echo canceller.

Bit 11: SAGC

Determines the gain of the AGC.

Bit 10: FSKen

Determines whether FSK or CAS/DTMF detector is enabled.

Table 19: ECP_CONTROL_REG address 1 (LSB)

value	7	6	5	4	3	2	1	0
			Format definition				ICLK	
0			000 = format 0 (Slave) 001 = format 1 (Master) 010 = format 2 (Slave) 011 = format 3 (Slave) 100 = format 4 (Master) 101 = format 5 (Master) 110 = format 6 (Slave)				External	divide by 1
1							Internal	divide by 2

Bits 5,4,3: Format definition

With these bits the interface formats for external devices can be defined (e.g. external codec, or ISDN devices, see previous chapters).

Bits 1,0: ICLK

With these bits the interface clock can be defined. The clock can be generated internally or accepted from an external device (in case of slave formats 0, 2, 3 and 6).

Table 20: RESET_INT_PENDING_REG1 (0.FF.02)

Bit	Mode	Symbol	Description	Reset
7	R/W	DIP_INT_PEND	Writing a 1 clears the pending DIP interrupt. If read the DIP interrupt status (pending/not pending) is returned.	0
6	R/W	CLK100_INT_PEND	Writing a 1 clears the pending Clock 100 interrupt. If read, the Clock 100 interrupt status (pending/not pending) is returned. See also DEBUG_REG[3]	0
5	R/W	TIM1_INT_PEND	Writing a 1 clears the pending Timer 1 interrupt. If read, the Timer 1 interrupt status (pending/not pending) is returned.	0
4	R/W	TIM0_INT_PEND	Writing a 1 clears the pending Timer 0 interrupt. If read, the Timer 0 interrupt status (pending/not pending) is returned.	0
3	R/W	SPI_INT_PEND	Writing a 1 clears the pending SPI interrupt. If read, the SPI interrupt status (pending/not pending) is returned.	0
2	R/W	UART_INT_PEND	Writing a 1 clears the pending UART interrupt. If read, the UART interrupt status (pending/not pending) is returned.	0
1	R/W	P10_INT_PEND	Writing a 1 clears the pending P10 interrupt. If read, the P10 interrupt status (pending/not pending) is returned.	0
0	R/W	KEYB_INT_PEND	Writing a 1 clears the pending Keyboard interrupt. If read, the Keyboard interrupt status (pending/not pending) is returned.	0

Table 21: RESET_INT_PENDING_REG2(0.FF.03)

BIT	MODE	SYMBOL	DESCRIPTION	RESET
7-2			-	
1	R/W	CLK8K_INT_PEND	Writing a 1 clears the pending CLK8K interrupt. If read the CLK8K_INT_PEND status is returned.	0
0	R/W	TONE_INT_PEND	Writing a 1 clears the pending TONE_INT interrupt. If read the TONE_INT_PEND status is returned.	0

Table 22: SET_INT_PENDING_REG1 (0.FF.04)

Bit	Mode	Symbol	Description	Reset
7	R/W	DIP_INT_PEND	If a DIP interrupt is generated this bit is set to 1. Writing a 1 will also generate a DIP interrupt. A 0 insertion is discarded. If read, the interrupt status (pending/not pending) is returned.	0
6	R/W	CLK100_INT_PEND	If a Clock 100 interrupt is generated this bit is set to 1. Writing a 1 will also generate a Clock 100 interrupt. A 0 insertion is discarded. If read, the interrupt status (pending/not pending) is returned. See also DEBUG_REG[3]	0
5	R/W	TIM1_INT_PEND	If a Timer 1interrupt is generated this bit is set to 1. Writing a 1 will also generate a Timer 1interrupt. A 0 insertion is discarded. If read, the interrupt status (pending/not pending) is returned.	0
4	R/W	TIM0_INT_PEND	If a Timer 0 interrupt is generated this bit is set to 1. Writing a 1 will also generate a Timer 0interrupt. A 0 insertion is discarded. If read, the interrupt status (pending/not pending) is returned.	0
3	R/W	SPI_INT_PEND	If a SPI interrupt is generated this bit is set to 1. Writing a 1 will also generate a SPI interrupt. A 0 insertion is discarded. If read, the interrupt status (pending/not pending) is returned.	0
2	R/W	UART_INT_PEND	If a UART interrupt is generated this bit is set to 1. Writing a 1 will also generate a UART interrupt. A 0 insertion is discarded. If read, the interrupt status (pending/not pending) is returned.	0
1	R/W	P10_INT_PEND	If a P10 interrupt is generated this bit is set to 1. Writing a 1 will also generate a P10 interrupt. A 0 insertion is discarded. If read, the interrupt status (pending/not pending) is returned.	0
0	R/W	KEYB_INT_PEND	If a Keyboard interrupt is generated this bit is set to 1. Writing a 1 will also generate a Keyboard interrupt. A 0 insertion is discarded. If read, the interrupt status (pending/not pending) is returned.	0

Table 23: SET_INT_PENDING_REG2(0.FF.05)

BIT	MODE	SYMBOL	DESCRIPTION	RESET
7-2			-	
1	R/W	CLK8K_INT_PEND	Set if the CLK8K_INT is generated. Writing a '1' will also generate the CLK8K_INT. If read the CLK8K_INT_PEND status is returned. This bit cleared in the RESET_INT_PEND_REG.	0
0	R/W	TONE_INT_PEND	Set if the TONE_INT is generated indicating that either an FSK byte is received or a DTMF tone, CAS tone or single tone is detected. Writing a '1' will also generate the TONE_INT. If read the TONE_INT_PEND status is returned. This bit cleared in the RESET_INT_PEND_REG.	0

Table 24: KEYB_INT_REG, P10_INT_REG, UART_INT_REG, SPI_INT_REG, TIM0_INT_REG, TIM1_INT_REG, CLK100_INT_REG, DIP_INT_REG, CLK8_INT_REG, TONE_INT_REG, (0.FF.04.. 0.FF.0A)

Address	Mode	Bits(6..4)	Bits(2..0)	Description	Reset
		PR_LEVEL[2..0]	**PR_LEVEL[2..0]**		0
0xFF06	R/W	DIP_INT_REG	CLK100_INT_REG	These bits define the priority level of a maskable interrupt. The maskable interrupt with the interrupt pending bit set (1) and the highest priority is serviced. After the interrupt is serviced the pending bit is NOT reset (0) by hardware.	0
0xFF07	R/W	TIM1_INT_REG	TIM0_INT_REG		0
0xFF08	R/W	SPI_INT_REG	UART_INT_REG		0
0xFF09	R/W	P10_INT_REG	KEYB_INT_REG		0
0xFF0A	R/W	CLK8_INT_REG	TONE_INT_REG	PR_LEVEL[2] PR_LEVEL[1] PR_LEVEL[0]:Priority 0 0 0 0 Disabled 0 0 1 1 Lowest 0 1 0 2 0 1 1 3 1 0 0 4 1 0 1 5 1 1 0 6 1 1 1 7 Highest The CLK100 interrupt is also disabled if the DIP clock is selected and the DIP is stopped. See DEBUG_REG[3]	0

Table 25: P0_IN_OUT_DATA_REG (0.FF.10)

Bit	Mode	Symbol	Description	Reset P0
7	R/W	P0_7_DATA	If output set P0[7], else returns the value of P0[7]	1
6	R/W	P0_6_DATA	If output set P0[6], else returns the value of P0[6]	0
5	R/W	P0_5_DATA	If output set P0[5], else returns the value of P0[5]	0
4	R/W	P0_4_DATA	If output set P0[4], else returns the value of P0[4]	1
3	R/W	P0_3_DATA	If output set P0[3], else returns the value of P0[3]	1
2	R/W	P0_2_DATA	If output set P0[2], else returns the value of P0[2]	1
1	R/W	P0_1_DATA	If output set P0[1], else returns the value of P0[1]	0
0	R/W	P0_0_DATA	If output set P0[0], else returns the value of P0[0]	0

NOTE: P0 bit 1,5,6 have pull down resistors. At reset these are activated. P0 bit 0,2,3,4,7 have pull up resistors. At reset all except P0[0] are activated

Table 26: P0_SET_OUTPUT_DATA_REG (0.FF.11)

Bit	Mode	Symbol	Description	Reset
7	W	P0_7_SET	If P0[7] output, writing a 1 sets P0[7] to 1. Writing 0 is discarded	0
6	W	P0_6_SET	If P0[6] output, writing a 1 sets P0[6] to 1. Writing 0 is discarded	0
5	W	P0_5_SET	If P0[5] output, writing a 1 sets P0[5] to 1. Writing 0 is discarded	0
4	W	P0_4_SET	If P0[4] output, writing a 1 sets P0[4] to 1. Writing 0 is discarded	0
3	W	P0_3_SET	If P0[3] output, writing a 1 sets P0[3] to 1. Writing 0 is discarded	0
2	W	P0_2_SET	If P0[2] output, writing a 1 sets P0[2] to 1. Writing 0 is discarded	0
1	W	P0_1_SET	If P0[1] output, writing a 1 sets P0[1] to 1. Writing 0 is discarded	0
0	W	P0_0_SET	If P0[0] output, writing a 1 sets P0[0] to 1. Writing 0 is discarded	0

Table 27: P0_RESET_OUTPUT_DATA_REG (0.FF.12)

Bit	Mode	Symbol	Description	Reset
7	W	P0_7_RESET	If P0[7] output, writing a 1 resets P0[7] to 0. Writing 0 is discarded	0
6	W	P0_6_RESET	If P0[6] output, writing a 1 resets P0[6] to 0. Writing 0 is discarded	0
5	W	P0_5_RESET	If P0[5] output, writing a 1 resets P0[5] to 0. Writing 0 is discarded	0
4	W	P0_4_RESET	If P0[4] output, writing a 1 resets P0[4] to 0. Writing 0 is discarded	0
3	W	P0_3_RESET	If P0[3] output, writing a 1 resets P0[3] to 0. Writing 0 is discarded	0
2	W	P0_2_RESET	If P0[2] output, writing a 1 resets P0[2] to 0. Writing 0 is discarded	0
1	W	P0_1_RESET	If P0[1] output, writing a 1 resets P0[1] to 0. Writing 0 is discarded	0
0	W	P0_0_RESET	If P0[0] output, writing a 1 resets P0[0] to 0. Writing 0 is discarded	0

Table 28: P0_DIR_REG (0.FF.13)

Bit	Mode	Symbol	Description	Reset
7	R/W	P0_7_DIR	If 1: P0[7] is output, if 0: P0[7] is input.	0
6	R/W	P0_6_DIR	If 1: P0[6] is output, if 0: P0[6] is input.	0
5	R/W	P0_5_DIR	If 1: P0[5] is output, if 0: P0[5] is input.	0
4	R/W	P0_4_DIR	If 1: P0[4] is output, if 0: P0[4] is input.	0
3	R/W	P0_3_DIR	If 1: P0[3] is output, if 0: P0[3] is input.	0
2	R/W	P0_2_DIR	If 1: P0[2] is output, if 0: P0[2] is input.	0
1	R/W	P0_1_DIR	If 1: P0[1] is output, if 0: P0[1] is input.	0
0	R/W	P0_0_DIR	If 1: P0[0] is output, if 0: P0[0] is input.	0
NOTE:	if P0[i] is set to input and output =1: pull up selected or output=0: pull down selected if available on the pin			

Table 29: P0_MODE_REG (0.FF.14)

Bit	Mode	Symbol	Description	Reset
7	R/W	ENCLK100	If 1 and P0_DIR_REG[7] is set to output, CLK100 is switched to pin P0[7]	0
6	R/W	ENAD19	If 1 and P0_DIR_REG[6] is set to output, AD19 is switched to pin P0[6]	0
5	R/W	ENREADY	If 1 READY is enabled and switched to pin P0[5].	0
4	R/W	ENCS2	If 1 and P0_DIR_REG[5] is set to output, CS2 is switched to pin P0[5]. Bit 5: READY must be '0'.	
3	R/W	ENCS1	If 1 and P0_DIR_REG[3] is set to output, CS1 is switched to pin P0[3]	0
2	R/W	ENCS0	If 1 and P0_DIR_REG[2] is set to output, CS0 is switched to pin P0[2]	0
0-1			Not used	

Note 1: To enable the TONE input, the P0_DIR_DIR[4] must be set to input.

Table 30: P0_CSMODE_REG (0.FF.15)

Bit	Mode	Symbol	Description	Reset
7	R/W	CS1_IOMODE	0 = Select IO expander mode for CS1. 1 = Select chip select mode	0
6	R/W	CS0_IOMODE	0 = Select IO expander mode for CS0. 1 = Select chip select mode	0
5-4	R/W	CS2_RWMODE	'00' generates a positive write pulse at CS2 if writing '01' generates a negative write pulse at CS2 if writing '10' generates a positive read pulse at CS2 if reading '11' generates a negative read pulse at CS2 if reading Active range is FF90-FF9F$_{16}$ (See Figure 4)	00
3-2	R/W	CS1_RWMODE	'00' generates a positive write pulse at CS1 if writing '01' generates a negative write pulse at CS1 if writing '10' generates a positive read pulse at CS1 if reading '11' generates a negative read pulse at CS1 if reading Active range is FF80-FF8F$_{16}$ (See Figure 4)	00
1-0	R/W	CS0_RWMODE	'00' generates a positive write pulse at CS0 if writing '01' generates a negative write pulse at CS0 if writing '10' generates a positive read pulse at CS0 if reading '11' generates a negative read pulse at CS0 if reading Active range is FF70-FF7F$_{16}$.(See Figure 4)	00

Note 2: CS2 is always in IO expander mode.

Table 31: P0_ENV_REG (0.FF.16)

Bit	Mode	Symbol	Description	Reset
7	R		Not used.	
6..5	R	test-mode	Internally used. P0[7] or P0[6] or P0[5] must be '0' at start-up.	P0[6..5]
4			Not used. (CR16B Core signals only available with 128 pins packages)	
3	R	APPL	Free environment bit for application use if TP = '0'	P0[3]
2	R	START	If '1' the application starts at 0$_{16}$, else the application starts at 10000$_{16}$	P0[2]
1	R	BOOT	If '1' the boot program loads a new application program from the UART and executes it from D800$_{16}$. If '0' the application starts from the address indicated by START. See also DEBUG_REG bit 4	P0[1]
0	R	-	Internally used.	P0[0]

NOTE: Test mode is only selected if TP (pin #50) =1.

Table 32: P0_TEST_CTRL_REG1(0.FF.17)

Bit	Mode	Symbol	Description	Reset
7-1	R/W	-	For test purpose only. Must be all 0 for normal operation	0
0			Not used	

Table 33: P0_TEST_CTRL_REG2(0.FF.18)

Bit	Mode	Symbol	Description	Reset
7-6	R/W	-	For test purpose only. Must be all 0 for normal operation	0
5			Not used	
4-0	R/W	-	For test purpose only. Must be all 0 for normal operation	0

Table 34: P0_UART_CTRL_REG (0.FF.19)

Bit	Mode	Symbol	Description	Reset
7	-	-	Not Used	-
6	R	RI	If 1 UART receive interrupt. Must be cleared by SW	0
5	R	TI	If 1 UART transmit interrupt. Must be cleared by SW	1
4	R/W	CLKSEL	If 1 the UART is clocked with 10.368 MHz. If 0 the UART is clocked with 1.152 MHz	0
3-2	R/W	BAUDRATE	UART baud rate selection: Bit4 = 0 Bit4 = 1 00 = 9600 Baud, 86.4 kBaud 01 = 19200 Baud, 172.8 kBaud 10 = 57.6 kBaud, 518.4 kBaud 11 = 115.2 kBaud 1036.8 kBaud	00
1	R/W	UART_TEN	If 1 the UART transmitter is enabled.	0
0	R/W	UART_REN	If 1 the UART receiver is enabled.	0

Table 35: P0_UART_RX_TX_REG (0.FF.1A)

Bit	Mode	Symbol	Description	Reset
7..0	R	UART_DATA	UART input register (RX)	00_{16}
	W		UART output register (TX)	

Table 36: P0_CLEAR_TX_INT_REG (0.FF.1B)

Bit	Mode	Symbol	Description	Reset
7..0	W	CLEAR_TX	Writing any value to this register will clear the UART TI interrupt	00_{16}

Table 37: P0_CLEAR_RX_INT_REG (0.FF.1C)

Bit	Mode	Symbol	Description	Reset
7..0	W	CLEAR_RX	Writing any value to this register will clear the UART RI interrupt	00_{16}

Table 38: P1_IN_OUT_DATA_REG (0.FF.20)

Bit	Mode	Symbol	Description	Reset
7	R/W	P1_7_DATA	If output set P1[7], else returns the value of P1[7]	1
6	R/W	P1_6_DATA	If output set P1[6], else returns the value of P1[6]	1
5	R/W	P1_5_DATA	If output set P1[5], else returns the value of P1[5]	1
4	R/W	P1_4_DATA	If output set P1[4], else returns the value of P1[4]	1
3	R/W	P1_3_DATA	If output set P1[3], else returns the value of P1[3]	1
2	R/W	P1_2_DATA	If output set P1[2], else returns the value of P1[2]	1
1	R/W	P1_1_DATA	If output set P1[1], else returns the value of P1[1]	1
0	R/W	P1_0_DATA	If output set P1[0], else returns the value of P1[0]	1

NOTE: P1 has pull up resistors. At reset P1 is input and pull-up resistors are activated.

Table 39: P1_SET_OUTPUT_DATA_REG (0.FF.21)

Bit	Mode	Symbol	Description	Reset
7	W	P1_7_SET	If P1[7] output, writing a 1 sets P1[7] to 1. Writing 0 is discarded	0
6	W	P1_6_SET	If P1[6] output, writing a 1 sets P1[6] to 1. Writing 0 is discarded	0
5	W	P1_5_SET	If P1[5] output, writing a 1 sets P1[5] to 1. Writing 0 is discarded	0
4	W	P1_4_SET	If P1[4] output, writing a 1 sets P1[4] to 1. Writing 0 is discarded	0
3	W	P1_3_SET	If P1[3] output, writing a 1 sets P1[3] to 1. Writing 0 is discarded	0
2	W	P1_2_SET	If P1[2] output, writing a 1 sets P1[2] to 1. Writing 0 is discarded	0
1	W	P1_1_SET	If P1[1] output, writing a 1 sets P1[1] to 1. Writing 0 is discarded	0
0	W	P1_0_SET	If P1[0] output, writing a 1 sets P1[0] to 1. Writing 0 is discarded	0

Table 40: P1_RESET_OUTPUT_DATA_REG (0.FF.22)

Bit	Mode	Symbol	Description	Reset
7	W	P1_7_RESET	If P1[7] output, writing a 1 resets P1[7] to 0. Writing 0 is discarded	0
6	W	P1_6_RESET	If P1[6] output, writing a 1 resets P1[6] to 0. Writing 0 is discarded	0
5	W	P1_5_RESET	If P1[5] output, writing a 1 resets P1[5] to 0. Writing 0 is discarded	0
4	W	P1_4_RESET	If P1[4] output, writing a 1 resets P1[4] to 0. Writing 0 is discarded	0
3	W	P1_3_RESET	If P1[3] output, writing a 1 resets P1[3] to 0. Writing 0 is discarded	0
2	W	P1_2_RESET	If P1[2] output, writing a 1 resets P1[2] to 0. Writing 0 is discarded	0
1	W	P1_1_RESET	If P1[1] output, writing a 1 resets P1[1] to 0. Writing 0 is discarded	0
0	W	P1_0_RESET	If P1[0] output, writing a 1 resets P1[0] to 0. Writing 0 is discarded	0

Table 41: P1_DIR_REG (0.FF.23)

Bit	Mode	Symbol	Description	Reset
7	R/W	P1_7_DIR	If 1: P1[7] is output, if 0: P1[7] is input.	0
6	R/W	P1_6_DIR	If 1: P1[6] is output, if 0: P1[6] is input.	0
5	R/W	P1_5_DIR	If 1: P1[5] is output, if 0: P1[5] is input.	0
4	R/W	P1_4_DIR	If 1: P1[4] is output, if 0: P1[4] is input.	0
3	R/W	P1_3_DIR	If 1: P1[3] is output, if 0: P1[3] is input.	0
2	R/W	P1_2_DIR	If 1: P1[2] is output, if 0: P1[2] is input.	0
1	R/W	P1_1_DIR	If 1: P1[1] is output, if 0: P1[1] is input.	0
0	R/W	P1_0_DIR	If 1: P1[0] is output, if 0: P1[0] is input.	0
NOTE:	if P1[i] is set to input and output =1: pull up selected or output=0: pull down selected if available on the pin			

Table 42: P1_MODE_REG (0.FF.24)

Bit	Mode	Symbol	Description	Reset
7	R/W	ENHOLD	If 1 and HOLDn = 0 then CR16 goes in HOLD mode. If 0 P1[7] has its normal bidirectional I/O function. If during the rising edge of RSTn P1[7] is LOW, the Emulation mode is entered and P1[7] becomes MI output.	0
6	R/W	ENACS	If 1 and P1_DIR_REG[6] is set to output, ACSn is switched to pin P1[6]	0
5	R/W	ENAD18	If 1 and P1_DIR_REG[5] is set to output, AD18 is switched to pin P1[5]	0
4-3	R/W		Not used	
2	R/W	SPIEN	'1': Enable SPI Operation.	0
1			Not used	
0	R/W	P10_LEVEL	If '0' generate interrupt if P1[0] = 0. If '1' generate interrupt if P1[0] = 1.	0

Table 43: P1_INT_EN_REG (0.FF.25)

Bit	Mode	Symbol	Description	Reset
7		P1[7]_INT_EN	If 1 the P1[7] interrupt is enabled	0
6		P1[6]_INT_EN	If 1 the P1[6] interrupt is enabled	0
5		P1[5]_INT_EN	If 1 the P1[5] interrupt is enabled	0
4		P1[4]_INT_EN	If 1 the P1[4] interrupt is enabled	0
3		P1[3]_INT_EN	If 1 the P1[3] interrupt is enabled	0
2		P1[2]_INT_EN	If 1 the P1[2] interrupt is enabled	0
1		P1[1]_INT_EN	If 1 the P1[1] interrupt is enabled	0
0		P1[0]_INT_EN	If 1 the P1[0] interrupt is enabled. If P10_INT is enabled and P1[0]_INT_EN = '1' then also KEY_INT is enabled.	0

Table 44: P1_DEBOUNCE_REG (0.FF.26)

Bit	Mode	Symbol	Description	Reset
7..3	-	-	Not Used	0
2..0	R/W	BOUNCE[2..0]	These bits define the keyboard debounce time. If P1[7..0] input is 0 the debounce time starts. If after debounce time (t) P1[7..0] is still low the keyboard interrupt pending bit is set to 1. BOUNCE[2] BOUNCE[1] BOUNCE[0]: Bounce Time 0 0 0 Disabled 0 0 1 0-10 msec 0 1 0 10-20 msec 0 1 1 20-30 msec 1 0 0 30-40 msec 1 0 1 40-50 msec 1 1 0 50-60 msec 1 1 1 60-70 msec.	0

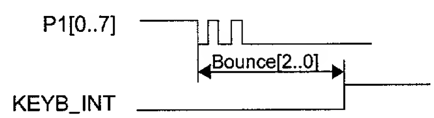


FIGURE 47. Keyboard Debounce Time

Table 45: P1_SPI_CTRL_REG (0.FF.27)

Bit	Mode	Symbol	Description	Reset
7..5	-	-	Not Used	0
4-3	R/W	SPICLK	Select SCK clock frequency in master mode: 00 = 576 kHz, 01 = 144k kHz, 10 = 72 kHz, 11 = 36 kHz	00
2	R/W	SPHA	Select SCK phase. See Table 12	0
1	R/W	SPOL	Select SCK polarity. If '1' SCK is initially high. See Table 12	0
0	R/W	SPI_MODE	If 1 the SPI is master. If 0 the SPI is Slave.	0
If applicable one or more P1_DIR_REG[1,2,3,4] bits must be set to '1' (= output) if SPI signals are output or master.				

Table 46: P1_SPI_RX_TX_REG (0.FF.28)

Bit	Mode	Symbol	Description	Reset
7..0	R	SPI_DATA	SPI input register	00_{16}
	W		SPI output register	

Table 47: P2_IN_OUT_DATA_REG (0.FF.30)

Bit	Mode	Symbol	Description	Reset
7	R/W	P2_7_DATA	If output set P2[7], else returns the value of P2[7]	0
6	R/W	P2_6_DATA	If output set P2[6], else returns the value of P2[6]	0
5	R/W	P2_5_DATA	If output set P2[5], else returns the value of P2[5]	0
4	R/W	P2_4_DATA	If output set P2[4], else returns the value of P2[4]	0
3	R/W	P2_3_DATA	If output set P2[3], else returns the value of P2[3]	0
2	R/W	P2_2_DATA	If output set P2[2], else returns the value of P2[2]	0
1	R/W	P2_1_DATA	If output set P2[1], else returns the value of P2[1]	0
0	R/W	P2_0_DATA	If output set P2[0], else returns the value of P2[0]	0

Table 48: P2_SET_OUTPUT_DATA_REG (0.FF.31)

Bit	Mode	Symbol	Description	Reset
7	W	P2_7_SET	If P2[7] output, writing a 1 sets P2[7] to 1. Writing 0 is discarded	0
6	W	P2_6_SET	If P2[6] output, writing a 1 sets P2[6] to 1. Writing 0 is discarded	0
5	W	P2_5_SET	If P2[5] output, writing a 1 sets P2[5] to 1. Writing 0 is discarded	0
4	W	P2_4_SET	If P2[4] output, writing a 1 sets P2[4] to 1. Writing 0 is discarded	0
3	W	P2_3_SET	If P2[3] output, writing a 1 sets P2[3] to 1. Writing 0 is discarded	0
2	W	P2_2_SET	If P2[2] output, writing a 1 sets P2[2] to 1. Writing 0 is discarded	0
1	W	P2_1_SET	If P2[1] output, writing a 1 sets P2[1] to 1. Writing 0 is discarded	0
0	W	P2_0_SET	If P2[0] output, writing a 1 sets P2[0] to 1. Writing 0 is discarded	0

Table 49: P2_RESET_OUTPUT_DATA_REG (0.FF.32)

Bit	Mode	Symbol	Description	Reset
7	W	P2_7_RESET	If P2[7] output, writing a 1 resets P2[7] to 0. Writing 0 is discarded	0
6	W	P2_6_RESET	If P2[6] output, writing a 1 resets P2[6] to 0. Writing 0 is discarded	0
5	W	P2_5_RESET	If P2[5] output, writing a 1 resets P2[5] to 0. Writing 0 is discarded	0
4	W	P2_4_RESET	If P2[4] output, writing a 1 resets P2[4] to 0. Writing 0 is discarded	0
3	W	P2_3_RESET	If P2[3] output, writing a 1 resets P2[3] to 0. Writing 0 is discarded	0
2	W	P2_2_RESET	If P2[2] output, writing a 1 resets P2[2] to 0. Writing 0 is discarded	0
1	W	P2_1_RESET	If P2[1] output, writing a 1 resets P2[1] to 0. Writing 0 is discarded	0
0	W	P2_0_RESET	If P2[0] output, writing a 1 resets P2[0] to 0. Writing 0 is discarded	0

Table 50: P2_DIR_REG (0.FF.33)

Bit	Mode	Symbol	Description	Reset
7	R/W	P2_7_DIR	If 1: P2[7] is output, if 0: P2[7] is input. (Note)	0
6	R/W	P2_6_DIR	If 1: P2[6] is output, if 0: P2[6] is input. (Note)	0
5	R/W	P2_5_DIR	If 1: P2[5] is output, if 0: P2[5] is input.	0
4	R/W	P2_4_DIR	If 1: P2[4] is output, if 0: P2[4] is input.	0
3	R/W	P2_3_DIR	If 1: P2[3] is output, if 0: P2[3] is input.	0
2	R/W	P2_2_DIR	If 1: P2[2] is output, if 0: P2[2] is input.	0
1	R/W	P2_1_DIR	If 1: P2[1] is output, if 0: P2[1] is input.	0
0	R/W	P2_0_DIR	If 1: P2[0] is output, if 0: P2[0] is input.	0
Note:	P2_6_DIR, P2_7_DIR output = digital, input = analog ADC0,1			

Table 51: P2_MODE_REG (0.FF.34)

Bit	Mode	Symbol	Description	Reset
7	R/W	HOLDACK_EN	If 1 and P2_DIR_REG[7] is set to output HOLDACK is enabled and switched to pin P2[7]	0
6-3	-	-	To enable ADC0, ADC2 and DAC0, P2_DIR_REG[6,7] must be set to input.	
2	R/W	PWM_EN	If '1' and P2_DIR_REG[2] = output then PWM timer 0 is swiched to P2[2]	0
1	R/W	STR1_EN	If 1 and P2_DIR_REG[1] is set to output STR1 is enabled and switched to pin P2[1]	0
0	R/W	CODEC_EN	If 1 STR0, ICLK, COUT, CIN and are switched to port P2 pins. If STR0 is output, P2_DIR_REG[0] must be set to output. If ICLK is output, P2_DIR_REG[3] must be set to output For the I/O function of CIN and COUT, P2_DIR[4] and P2_DIR_[5] must always be set to input.	0

Table 52: AD_CTRL_REG (0.FF.40)

Bit	Mode	Symbol	Description	Reset
7-4	R/W	-	Internally used. Bit 4 must be '0' for normal operation.	0
3-2	R/W	ADC_SEL[3-2]	Select ADC input: 00 = Select ADC0 01 = Select ADC1 10 = Select ADC2 11 = Switch ADC_DAC to ADC0 pin and disable all ADC functions. Note that P2_DIR_REG[6,7] must be '0' to disabled outputs.	00
1	R/W	DAC_PD	If '0' DAC is enabled, if '1' the DAC is switched off and DAC pin = '1'.	0
0	R/W	ADC_START	If 1 ADC starts conversion. After conversion this bit is set to 0	0

Table 53: ADC_REG (0.FF.41)

Bit	Mode	Symbol	Description	Reset
7..0	R/W	ADC_DAC	Read: Returns the value of the last ADC conversion. Write: If ADC_SEL = 11 then write ADC_DAC value, output on ADC0 pin and P2_DIR_REG[6] is set to input.	80_{16}

Table 54: DAC_REG (0.FF.42)

Bit	Mode	Symbol	Description	Reset
7..0	RW	DAC_VAL	DAC conversion value, output on DAC pin	80_{16}

Table 55: DAC2_REG (0.FF.43)

Bit	Mode	Symbol	Description	Reset
7..0	RW	DAC2_VAL	DAC conversion value, output on DAC2 pin	80_{16}

Table 56: TONE_MUX_REG1 (0.FF.44)

Bit	Mode	Symbol	Description	Reset
7..4	RW	TIMER_RELOAD	Select clock divider reload value for clock to latch timer periodically 0 = divide by 1, 15 = divide by 16	0000
3-2	RW	CLKSRC	00 = 144 kHz 01 = TONE input 10 = ECZ 11 = EZC2	0
1-0	RW	GATESRC	00 = 98Hz 01 = P1.0 input 10 = ECZ 11 = EZC2	0

Table 57: TONE_MUX_REG2 (0.FF.45)

Bit	Mode	Symbol	Description	Reset
7..4	RW	TIMER_RELOAD2	Select clock divider reload value for clock to latch timer periodically. 0 = divide by 1, 15 = divide by 16	0000
3-2	RW	CLKSRC2	00 = 144 kHz 01 = TONE input 10 = ECZ 11 = EZC2	0
1-0	RW	GATESRC2	00 = 98Hz 01 = P1.0 input 10 = ECZ 11 = EZC2	0

Table 58: TONE_COUNTER_REG1 (0.FF.46 0.FF.47)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0.FF.47								0.FF.46							

Bit	Mode	Symbol	Description	Reset
15..0	R	TONE_COUNTER	The TONE_COUNTER counts continuously with a selectable clock source. Sources are selected with CLKSRC values in the TONE_MUX_REG. Periodically the counter is latched in TONE_LATCH_REG	0000_{16}

Table 59: TONE_LATCH_REG1 (0.FF.48 0.FF.49)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0.FF.49								0.FF.48							

Bit	Mode	Symbol	Description	Reset
15..0	R	TONE_LATCH	Contains the latched TONE_COUNTER value	0000_{16}

Table 60: TONE_COUNTER_REG2 (0.FF.4A 0.FF.4B)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0.FF.4B								0.FF.4A							

Bit	Mode	Symbol	Description	Reset
15..0	R	TONE_COUNTER 2	The TONE_COUNTER2 counts continuously with a selectable clock source. Sources are selected with CLKSRC2 values in the TONE_MUX_REG2. Periodically the counter is latched in TONE_LATCH_REG2	0000_{16}

Table 61: TONE_LATCH_REG2 (0.FF.4C 0.FF.4D)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0.FF.4D								0.FF.4C							

Bit	Mode	Symbol	Description	Reset
15..0	R	TONE_LATCH2	Contains the latched TONE_COUNTER2 value	0000_{16}

Table 62: TIMER0_RELOAD_M_REG (0.FF.52, 0.FF.53)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0.FF.53								0.FF.52							

Bit	Mode	Symbol	Description	Reset
15 .. 0	R/W	TIM0_M	Timer 0 'high' reload value: Timer cycle = $(1/f_l)*((M+1)+(N+1))[s]$ Timer "H" = $(1/f_l)*((M+1)[s]$ f_l = 1.152MHz or 10.368 MHz If read, the actual counter value is returned	0000_{16}

Table 63: TIMER0_RELOAD_N_REG (0.FF.54, 0.FF.55)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0.FF.55								0.FF.54							

Bit	Mode	Symbol	Description	Reset
15 .. 0	R/W	TIM0_N	Timer 0 ‘low’ reload value: Timer cycle = $(1/f_i)*((M+1)+(N+1))[s]$ Timer “H” = $(1/f_i)*((M+1)[s]$ f_i = 1.152MHz or 10.368 MHz If read, the actual counter value is returned	0000_{16}

Table 64: TIMER1_RELOAD_M_REG (0.FF.56, 0.FF.57)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0.FF.57								0.FF.56							

Bit	Mode	Symbol	Description	Reset
15 .. 0	W	TIM1_M	Timer 1 ‘high’ reload value: Timer cycle = $(1/f_i)*((M+1)+(N+1))[s]$ Timer “H” = $(1/f_i)*((M+1)[s]$ f_i = 1.152MHz If read, the actual counter value is returned	0000_{16}

Table 65: TIMER1_RELOAD_N_REG (0.FF.58, 0.FF.59)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0.FF.59								0.FF.58							

Bit	Mode	Symbol	Description	Reset
15 .. 0	W	TIM1_N	Timer 1 ‘low’ reload value: Timer cycle = $(1/f_i)*((M+1)+(N+1))[s]$ Timer “H” = $(1/f_i)*((M+1)[s]$ f_i = 1.152MHz If read, the actual counter value is returned	0000_{16}

Table 66: TIMER_CTRL_REG (0.FF.5A)

Bit	Mode	Symbol	Description	Reset
7-5	R/W	-	-	
4-3	R/W		Must be 0 for proper operation	0
2	R/W	CLK_SEL	if 0, TIMER0 Clock input is 1.152 MHz If 1, TIMER0 Clock input is 10.368 MHz	0
1	R/W	TIM1_CTRL	If 1 timer 1 is running	0
0	R/W	TIM0_CTRL	If 1 timer 0 is running	0

Table 67: **CLK_DIV_REG (0.FF.60))**

Bit	Mode	Symbol	Description	Reset
7..3	-	-	Not Used	0
2..0	R/W	CLK_DIV[2..0]	System clock divider. CLK_DIV[2] CLK_DIV[1] CLK_DIV[0]: Divide by: 0 0 0 8 0 0 1 1 0 1 0 2 0 1 1 3 1 0 0 4 1 0 1 5 1 1 0 6 1 1 1 7	0

Table 68: **AUX_CS_LOW_REG (0.FF.62)**

Bit	Mode	Symbol	Description	Reset
7..0	R/W	AUX_LOW	If (AD[19..12] pins >= AUX_LOW[7..0]) and (AD[19..12] pins < AUX_HIGH[7..0]) and (AUX_HIGH[7..0] <> 0) then ACSn = 0 and RCSn = 1	00_{16}

Table 69: **AUX_CS_HIGH_REG (0.FF.63)**

Bit	Mode	Symbol	Description	Reset
7..0	R/W	AUX_HIGH	If (AD[19..12] pins < AUX_HIGH[7..0]) and (AD[19..12] pins >= AUX_LOW[7..0]) and (AUX_HIGH[7..0] <> 0) then ACSn = 0 and RCSn = 1	00_{16}

Table 70: **AUX_WAIT_REG (0.FF.64)**

Bit	Mode	Symbol	Description	Reset
7..3	-	-	Not Used	0
2..0	R/W	AUX_WAIT	Auxiliary wait cycles AUX_WAIT[2] AUX_WAIT[1] AUX_WAIT[0]: # wait cycles: 0 0 0 0 0 0 1 1 0 1 0 2 0 1 1 3 1 0 0 4 1 0 1 5 1 1 0 6 1 1 1 7	0

Table 71: SET_FREEZE_REG (0.FF.65)

Bit	Mode	Symbol	Description	Reset
7..4	-	-	Not Used	0
3	R/W	FRZ_WDOG	If 1 the watchdog timer is frozen. 0 is discarded	0
2	R/W	FRZ_TIM1	If 1 timer 1 is frozen. 0 is discarded	0
1	R/W	FRZ_TIM0	If 1 timer 0 is frozen. 0 is discarded	0
0	R/W	FRZ_DIP	If 1 the DIP is frozen. 0 is discarded	0

Table 72: RESET_FREEZE_REG (0.FF.66)

Bit	Mode	Symbol	Description	Reset
7..4	-	-	Not Used	0
3	R/W	FRZ_WDOG	If 1 the watchdog timer continues. 0 is discarded	0
2	R/W	FRZ_TIM1	If 1 timer 1 continues. 0 is discarded	0
1	R/W	FRZ_TIM0	If 1 timer 0 continues. 0 is discarded	0
0	R/W	FRZ_DIP	If 1 the DIP continues. 0 is discarded	0

Table 73: DEBUG_REG (0.FF.67)

Bit	Mode	Symbol	Description	Reset
7			Not used	
6			Not used	
5	R/W	DIS_BOOT	'0' Internal boot ROM is enabled '1' Internal boot ROM is disabled.	NOTE
4	R/W	ENV_B1	If 1 the P0_ENV_REG bit 1 is set to 0. This disables the loading of a new program after software reset.	NOTE
3	R/W	CLK100_SRC	If 1 the CLK100 interrupt source is a continuous 10.66 msec clock. If 0 the DIP 10 msec clock is used. If the DIP is stopped no CLK100 interrupts are generated.	0
2			Not used	
1	R/W	SW_RESET	If 1 the SC14424 puts all its on chip peripherals and registers in the reset state and CR16B starts executing at address 0. ENV_REG and DEBUG_REG[4,5,6] are only cleared after RSTN.	0
0	R/W	EN_BUS	If 1 the AD[19..0], DAB[7..0], RDn and WRn pins are always active. This allows tracing of the System Bus by an external processor. If 0 the AD[17..0], DAB[7..0], RDn and WRn pins are ONLY active during ACSn = 0 or RCSn = 0.RDn and WRn pins are set to 1	0
NOTE: set to 0 **ONLY** after RSTn				

Table 74: WATCHDOG_REG (0.FF.68)

Bit	Mode	Symbol	Description	Reset
7..0	R/W	WDOG_VAL	Watchdog preset value. Decremented by 1 every 10msec. If 0 a NMI interrupt is generated and FF_{16}.is automatically reloaded.	FF_{16}

Table 75: DIP_CTRL_REG (0.FF.E2)

BIT	MODE	SYMBOL	DESCRIPTION	RESET
7	R/W	URST	If this bit is set to 0 the DIP starts executing the DIP sequencer program. The first DIP instruction executed is located at address 0.FA.02. Writing a 1 to this bit stops the DIP sequencer program execution.	1
6	R/W	PRESCALER	Xtal clock prescaler. If set to 1 and the DIP executes the <U_PSC> command the Xtal1 clock (10.368MHz) is divided by 16 before it is passed on to the CR16B. The prescaler is switched off if this bit is set to 0 or one of the <U_INTx> DIP commands is executed.	0
5	R/W	DIP_BRK_INT	If the DIP <BRK> command is executed the DIP stops executing the sequencer program and sets DIP_BRK_INT to 1. Also the DIP_INT_PEND in SET/RESET_INT_R is set to 1. The DIP_BRK_INT bit is cleared on reading. Writing a 1 to it starts DIP program execution at the location where the <BRK> command was located.	0
4	R/W	ECP_INT	Read: '1' ONOFF_TIMER is expired. This bit is cleared if DIP_CTRL_REG is read. It also sets the DIP_INT_PEND. Write: '0' Disable ECP_INT, '1' Enable ECP_INT.	0
3-0	RO	DIP_INT_VEC[3-0]	If the DIP <U_INTx> (x = 0..3) command is executed on of the bits 3-0 are set and the DIP interrupt pending is set to 1.The DIP <U_VINT> command sets a four bits vectors. Reading this bits sets this bit to 0 and the DIP interrupt pending bit is also set to 0.	0

Note 3: The DIP_STATUS_REG is identical to DIP_CTRL_REG. If read, the DIP_INT the interrupt. is not cleared

5.0 Specifications

Table 76: Absolute maximum ratings (Note 4)

Parameter	Min	Max	Units
Power supply voltage (VDD-VSS / AVD-AVS)		3.6	V
Voltage on all digital inputs	VSS-0.3	5.25	V
Voltage on other pins	VSS-0.3	VDD+0.3	V
Storage temperature	-65	+150	°C
Package power dissipation @ 25 °C		500	mW

Note 4: Absolute maximum ratings are those values beyond which damage to the device may occur

Table 77: Operating conditions

Parameter	Description	Min	Typ	Max	Units
TA	Ambient temperature (Note 5)	-10		60	°C
VDD,AVD,AVD2, VDDRF	Positive supply voltage (Note 6, 7)	2.7	3.0	3.3	V
Xclk	Crystal frequency (Note 8)		10.368		MHz

Note 5: Within this temperature range full operation is guaranteed.

Note 6: Functional operation is guaranteed with VDD AVD up to 3.3V.

Note 7: The differences between AVD, VDD may never be more than 300mV, during a short period of time e.g. during power up more than 300mV difference is allowed.

Note 8: CLK_DIV_REG = '0'.

5.1 PIN TYPE DEFINITIONS

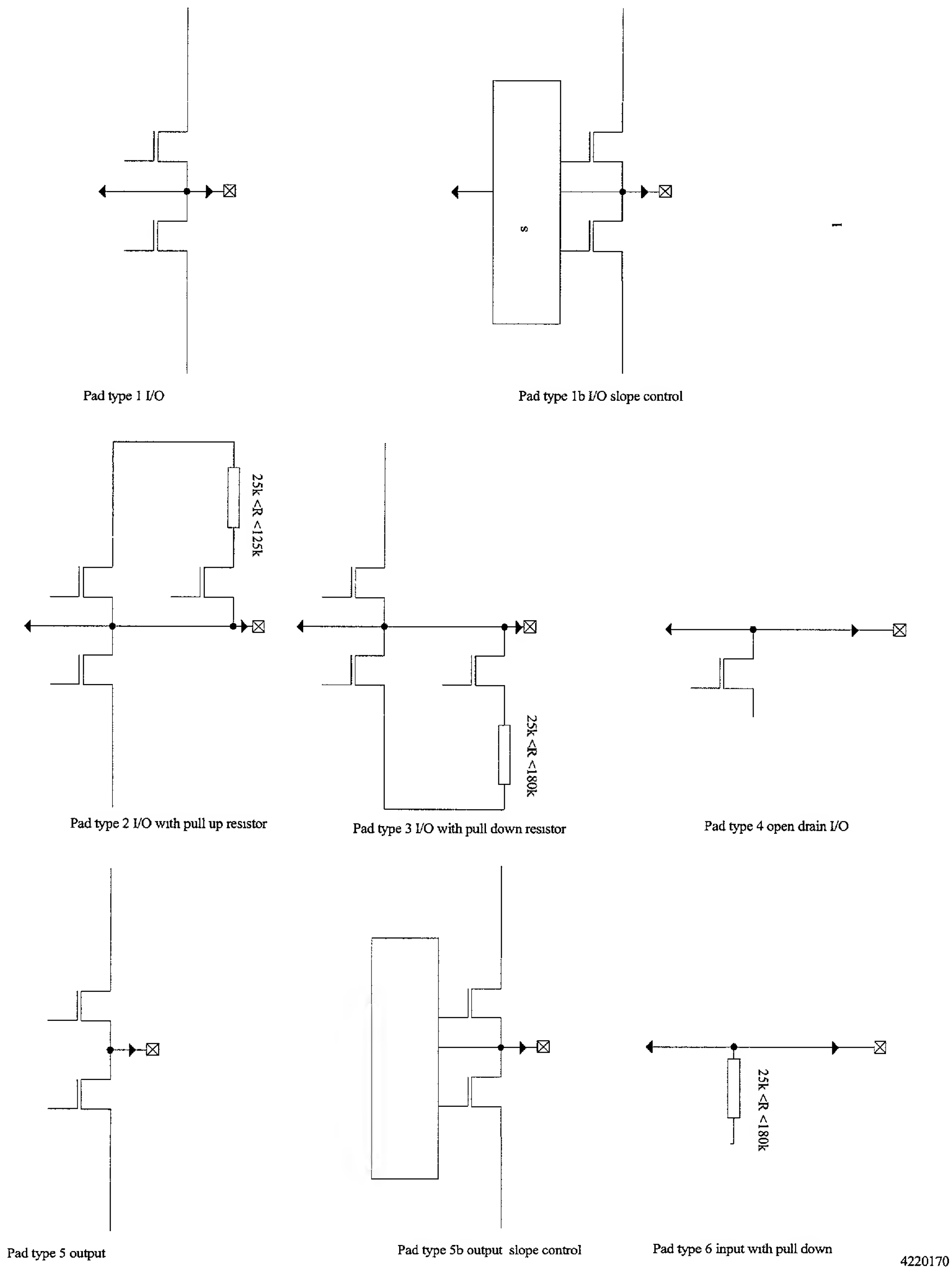


FIGURE 48. Pin type definitions

5.2 ELECTRICAL CHARACTERISTICS

VDD, AVD, VDD2 = 3.0 Volt all signals are related to V_{SS}, T_A = -10°C - +60 °C, crystal frequency = 10.368 MHz

Table 78: Supply currents

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
I_{VDD}	Digital supply current (pin 2 + pin 39)	Duplex voice/data connection, ADPCM channel 0, codec and encryption on. CR16 clock at div 8, prescaler on, TDO in gaussian mode. Active ECP block. One full slot active, 6 bits DAC on, Peak hold ADC on. No load on LRSM/LRSP, No load on TDO.		6		mA
	CompactRISC™ core (Note 9); CR16 + SBI + ICU + RAM/ROM			0.5		mA/ MHz
I_{AVD}	Analog supply current (pin 18)			400		µA
I_{AVD2}	Analog supply current (pin 64)			1.6		mA
I_{VDDRF}	Analog supply current (pin 12)	Xtal connected RF. RFCLK disabled		0.33		mA
I_{VDD}		Paging mode • One active receive channel every 16 frames (Paging mode) • RF-clock disabled • UCLK = 81 kHz • Crystal connected		1.7		mA
I_{AVD}				350		µA
I_{AVD2}				0		µA
ΔI_{VDD}	Increase of digital supply current (pin 2+ pin 49)	Second ADPCM channel active + N additional active slots full duplex (N<12) with encryption.		2.0 + N*200		mA µA
ΔI_{AVD}	Increase of analog supply current			20		µA
ΔI_{AVD2}	Increase of analog supply current 2			0		µA

Note 9: Refer to chapter 4.3. System Clock generation

Table 79: Digital inputs and I/Os

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
V_{IL}	Logic 0 input level				0.2*VDD	V
V_{IH}	Logic 1 input level		0.7*VDD			V
I_{in}	Input current	All inputs, except for HOLDn (Fixed internal pull up) P0,P1 (Internal pull up note 10,11) Vin = VDD Vin = VSS P0 (internal pull down note 10,11) Vin = VDD Vin = VSS	 15 15 		10 10 100 100 10	µA µA µA µA µA

Note 10: P0[i], P1[i] and P2[i] port pins are selected as input if P0,1,2_DIR_REG[i] = '0'.

Note 11: Internal pull-up resistors are selected if P0,1_OUTPUT_DATA[i] = '1'; Internal pull-down resistors are selected if P0_OUTPUT_DATA[i] = '0'.

Table 80: Digital outputs

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OL}	Logic 0 output level	I_{OUT} as specified below			0.5	V
V_{OH}	Logic 1 output level	I_{OUT} as specified below	VDD-0.5			V
I_{out}	Output current	P2[2] (Note 12) PD5,6,7, TDO, P1[4:0] All other outputs	100 12 2			mA mA mA

Note 12: Open collector outputs. The maximum voltage on these pins may not exceed VDD

Table 81: General purpose ADC. The input is multiplexed to ADC(0..2)

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
	Resolution			8		bits
	Conversion time				56	µsec
V_{in}	input range		0		AVD2	V
Non-linearity	Differential				±0.5	LSB
	Integral				±2	LSB
Rsource	Input impedance				350 k	MΩ
Cin	Input capacitance				5	pF
Voffset	Offset Voltage				0.5	LSB

Table 82: General purpose DAC, DAC2 (pin 63, 16)

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
	Resolution			8		bits
V_{out}		DAC_REG[7:0]=00_{16}		AVS		V
		DAC_REG[7:0]=FF_{16}		AVD		V

Table 82: General purpose DAC, DAC2 (pin 63, 16)

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
Non-linearity	Differential				±0.5	LSB
	Integral				±2	LSB
Rload	Minimum load impedance		0		220	kΩ
Cload	maximum capacitive load				30	pF

Table 83: Peak Hold ADC (pin 19)

Parameter	Description	Conditions	Min	Typ	Max	Units
	Resolution			6		bits
	Conversion time				32	µsec
V_{in}	Low level on RSSI pin	ADC[5:0]=00(hex)	0.06*AVD	0.086*AVD	0.11*AVD	V
	High level on RSSI pin	ADC[5:0]=3F(hex)	0.48*AVD	0.5*AVD	0.52*AVD	V
Non-linearity	Differential				±0.5	LSB
	Integral				±1	LSB
Rin	Input impedance	PD0 = '0'	1			MΩ
		PD0 = '1'			5	kΩ

Table 84: CMPREF DAC (pin 18)

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
	Resolution			6		bits
V_{out}	Low level on CMPREF	DAC[7:0]=00(hex) DON='1'	0.39* AVD	0.67* AVD	0.44* AVD	V
	High level on CMPREF	DAC[7:0]=FF(hex) DON='1'	0.56* AVD	0.33* AVD	0.61* AVD	V
Non-linearity	Differential				±0.5	LSB
	Integral				±2	LSB

Table 85: RDI - Comparator (pin 17)

Parameter	Description	Conditions	Min	Typ	Max	Units
V_{offset}	Input offset voltage		-10		10	mV
I_{in}	Input current	V_{IN} = 2.5 V on both RDI and CMPREF (DON = '0')	-100	1	100	nA
Vin	Input range		0		1.72	nA

5.3 TIMING CHARACTERISTICS

Table 86: RSTn PIN

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
t_{LOW}	Minimum low time to reset device	After power up.	10			msec
		In active mode (Note 13)	100			nsec

Note 13: spikes down to 5 nsec may reset the device

Table 87: EXTERNAL CLOCK on XTAL1

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
f	Input signal frequency				10.4	MHz
t_{LOW}	Duty cycle		40		60	%
V_{IL}	Logic 0 input Level				0.2*AVD	V
V_{IH}	Logic 1 input level		0.7*AVD			V
		Minimum current consumption	0.9*AVD			V

Table 88: RFCLK

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
1 / t_{PERIOD}	RFCLK Frequency			10368		kHz
t_{LOW}	RFCLK duty cycle		40		60	%
Phase Noise		250 Hz from carrier		-136		dBc

Table 89: RDI -CMPREF

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
t_{HOLD}	RDI hold time from rising edge RCK	CMPREF level as specified (V_{in}) with 50mV overdrive. (VIL,VIH)	0			nsec
t_{SETUP}	RDI setup time to rising edge RCK		40			nsec
V_{in}	V_{in}		1.25		AVD - 0.5	V

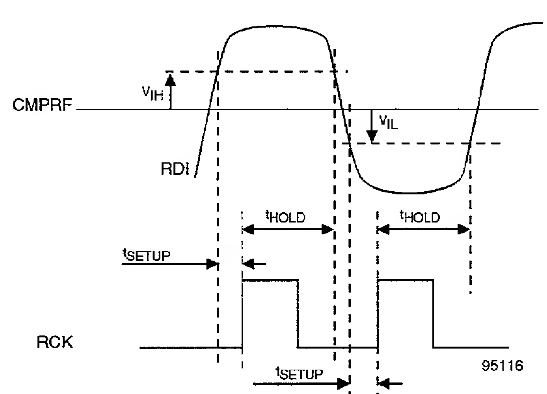


FIGURE 49. RDI Timing diagram

Table 90: MICROWIRE interface (max 50 pF load on all outputs)

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
Tres	MEN1n Switching accuracy			1/1.152		µsec
F_{SK}	SK frequency			1.152		MHz
$t_{FK\text{-}HIGH}$	SK high time		300			nsec
t_{RF}	SO	relative to falling edge SK	-25		25	nsec

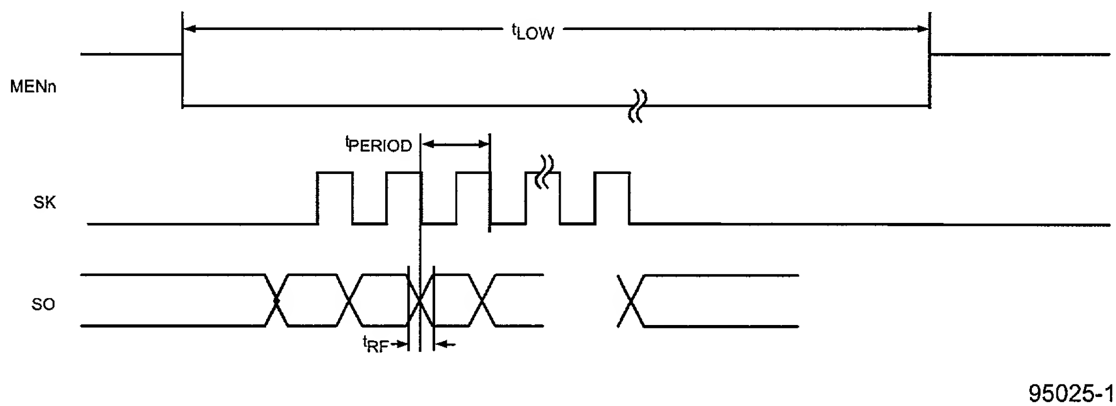


FIGURE 50. Micro wire timing diagram (default mode)

Table 91: PD(7..1) pins

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
Tres	PD(7..0) Switching accuracy	PD(7-1) externally available, PD0 internally connected to RSSI ADC		1/1.152		µsec

Table 92: TDO pin, digital mode M[1:0] = '00'

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
I_{out}	Output current		12			mA
VOL	Logic 0 output level				0.5	V
VOH	Logic 1 output level		VDD-0.5			V

Table 93: TDO pin, Gaussian mode M[1:0] = '01'

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
R_{load}	Load resistance		5			kΩ
$C_{parasitic}$	Load capacitance				20	pF
Rout	Output impedance				50	Ω
V_{out}	Output level (Note 14)	At 0dB level (VOL[5:0]=32), 0101010....-pattern	0.53	0.59	0.65	V_{pp}
$V_{out-max}$	Maximum output level	at 0dB level (VOL[5:0]=32), 111000111000....-pattern	0.64	0.67	0.71	V_{pp}
$V_{out-adj}$	Output level adjustment	6 bits tuning	-6		+6	dB
Vmid	Mid level		1.15	1.225	1.35	V
SINAD		f=1.152/2 for max level		40		dB

Note 14: V_{out} is independent of supply voltage

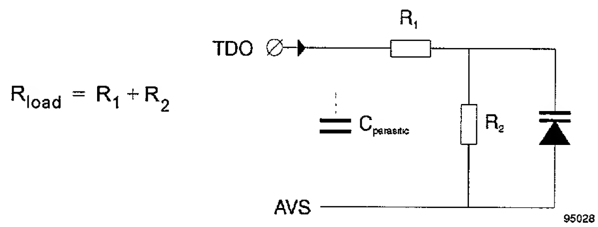


FIGURE 51. Typical application of TDO output in gaussian mode

Table 94: TDO pin, Mid Level mode [1:0] = '11'

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
V_{out}	Output level			1.225		V

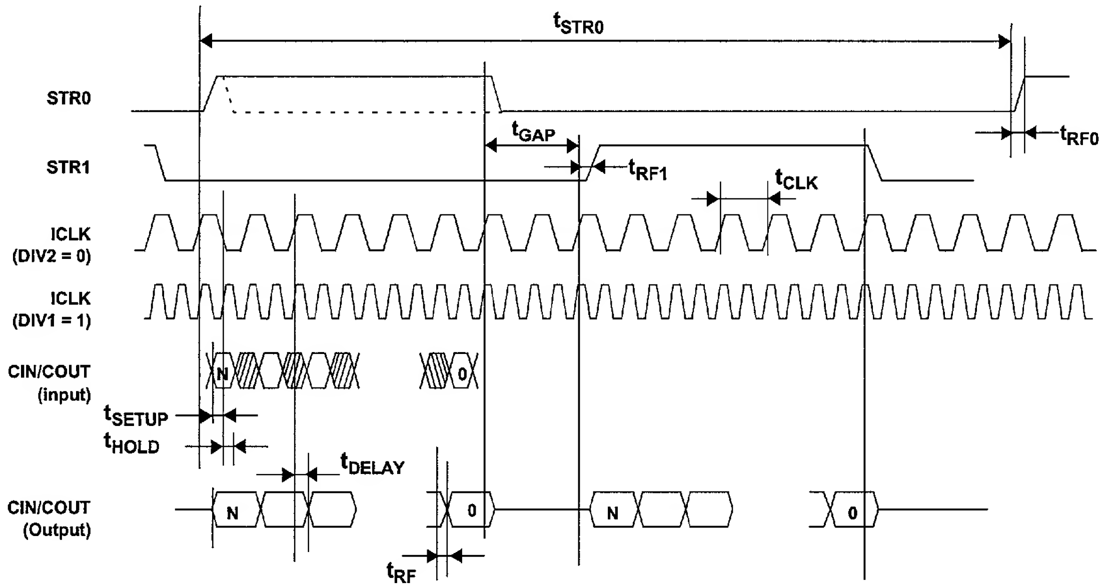


FIGURE 52. ECP/CODEC Interface timing diagram

Table 95: ECP/CODEC interface timing characteristics (max 50 pF load on all outputs)

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
t_{SETUP}	COUT, CIN input setup time	Relative to falling edge of ICLK	25			nsec
t_{HOLD}	COUT, CIN input hold time	Relative to falling edge of ICLK	25			nsec
t_{DELAY}	CIN, COUT output delay times	Relative to rising edge of ICLK			10	nsec
t_{RF}	CIN, COUT output rise/ fall time		-25		25	nsec
$1/t_{CLK}$	ICLK frequency	format 0,2,3,6				
		- div1	512		2048	kHz
		- div2	1024		4096	kHz
		format 1,4,5				
		- div1	2304		2304	kHz
		- div2	1152		1152	kHz
t_{STR0}	STR0 Repetition rate		8		8	kHz

Table 95: ECP/CODEC interface timing characteristics (max 50 pF load on all outputs)

t_{HIGH0}	STR0 duration	div1 (Note 15)				
		format 0	1			ICLK cycles
		format 1	8		8	ICLK cycles
		format 2	1			ICLK cycles
		format 3	1			ICLK cycles
		format 4	16		16	ICLK cycles
		format 5	16		16	ICLK cycles
		format 6	1			ICLK cycles
t_{RF0}	STR0 rise/fall times	format 1,4,5	-25		+25	nsec
t_{STR1}	STR1 Repetition rate	format 0, 2, 3, 6	0		8	kHz
t_{HIGH1}	STR1 duration	div1 (Note 15)				
		format 0	16		32	ICLK cycles
		format 1	16		16	ICLK cycles
		format 2	8		24	ICLK cycles
		format 3	0		16	ICLK cycles
		format 4	16		16	ICLK cycles
		format 5	16		16 + 16	ICLK cycles
		format 6	0		16	ICLK cycles
t_{RF1}	STR1 rise/fall times	format1	-25		+25	nsec
t_{GAP}	STR0, STR1	div1 (Note 15)				
		format 1,4,5	8		8	ICLK cycles
		format 2, 3,6	2			ICLK cycles

Note 15: If div2 is selected the given number of ICLK cycles must be multiplied by 2.

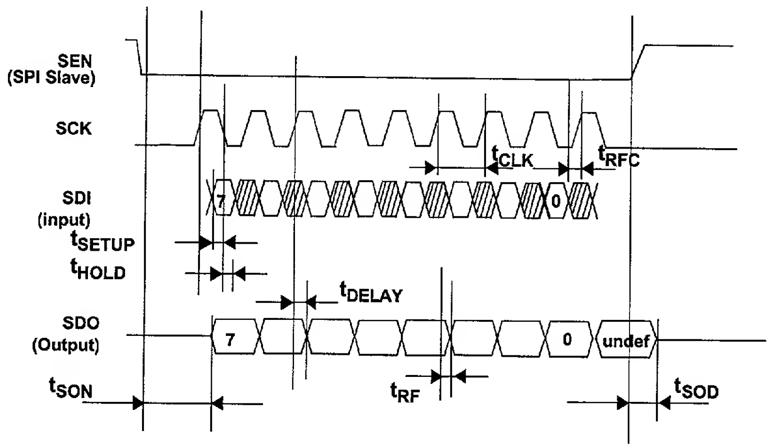


FIGURE 53. SPI Interface timing diagram

Table 96: SPI interface timing characteristics (max 50 pF load on all outputs)

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
t_{SON}	SDO enable time	SPI Slave	10			nsec
t_{SOD}	SDO disable time	SPI Slave	10			nsec
t_{SETUP}	SDI setup time	Relative to falling edge of SCK	25			nsec
t_{HOLD}	SDI hold time	Relative to falling edge of SCK	25			nsec
t_{DELAY}	SDO output delay time	Relative to rising edge of SCK			20	nsec
t_{RF}	SDO output rise/ fall time		-25		25	nsec
$1/t_{CLK}$	SCK Frequency	SPI master				
		SPI_MODE = 11		36		kHz
		SPI_MODE = 10		72		kHz
		SPI_MODE = 01		144		kHz
		SPI_MODE = 00		576		kHz
		SPI slave			1	MHz
t_{RFC}	SCK output rise/ fall time		-25		25	nsec
t_{SSETUP}	SEN to SCK active	SPI Slave mode	25			nsec
t_{SHOLD}	SCK to SEN inactive	SPI Slave mode	25			nsec

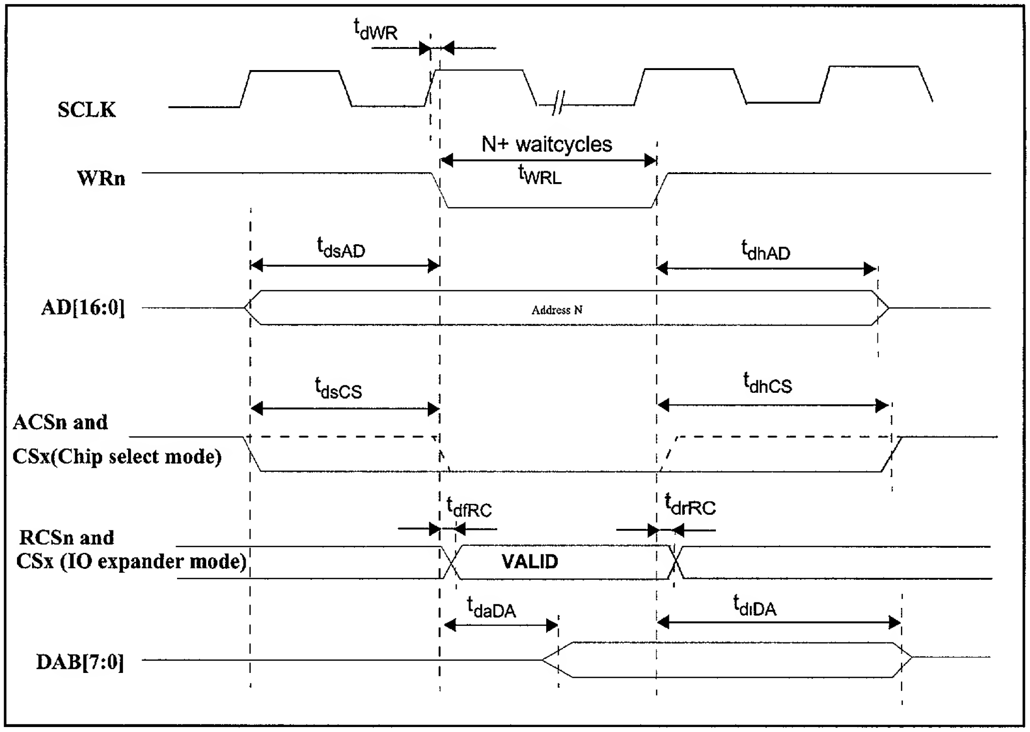


FIGURE 54. Write cycle timing diagram (HOLDn = '1')

Table 97: Timing characteristics for the SBI Interface write cycle (T=85°C, VDD = 2.7V, max. load = 30pF)

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
t_{dWR}	SCLK time to WRN				10	nsec
t_{WRL}	WRN Low period	Clock division ratio = N	N*96-5	N*96		nsec
t_{dsAD}	AD[0:16] time to WRn		N*96-10		N*96+10	nsec
t_{dhAD}	WRn to AD[0:16]		N*96-10		N*96+10	nsec
t_{dsCS}	ACSn time to WRN		N*96-5		N*96+5	nsec
t_{dhCS}	WRn time to ACSn		N*96-5		N*96+5	nsec
t_{dsCS}	CSx time to WRN	CS in Chip select mode	N*96-5		N*96+5	nsec
t_{dhCS}	WRN time to CSn	CS in Chip select mode	N*96-5		N*96+5	nsec
t_{dfRC}	WRN time to RCSn		-5		5	nsec
t_{drRC}	WRN time to RCSn		-5		5	nsec
t_{dfRC}	WRN time to CSx	CSx in I/O exp mode	-5		10	nsec
t_{drRC}	WRn time to CSx	CSx in I/O exp mode	-5		10	nsec
t_{daDA}	WRN time to DAB[7:0] stable				20	nsec
t_{diDA}	WRN time to DAB[7:0] 3-state		N*96 -10			nsec

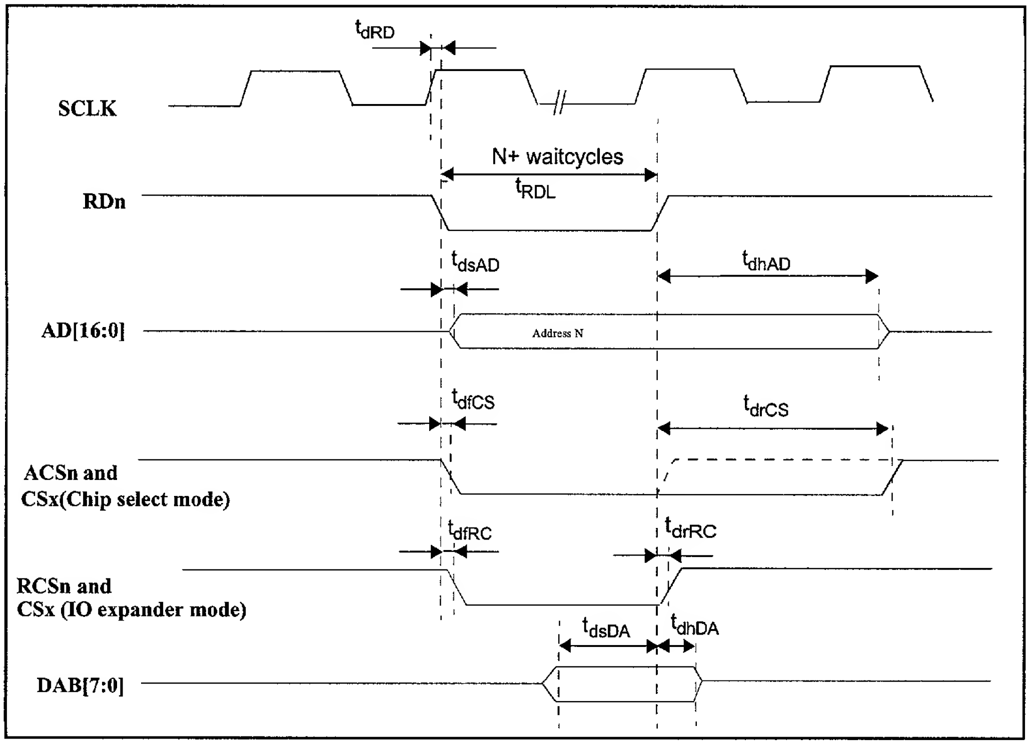


FIGURE 55. Read cycle timing diagram (HOLDn = '1')

Table 98: Timing characteristics for the SBI Interface read cycle (T=85°C, VDD = 2.7V, max. load = 30pF)

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
t_{dRD}	SCLK time to RDn				10	nsec
t_{RDL}	RDN Low period	Clock division N=1,2,3	N*96-5	N*96		nsec
		Clock division N >3 During RCS access	3*96-5	3*96		nsec
t_{dsAD}	AD[0:16] time to RDn		-5		5	nsec
t_{dhAD}	RDn time to AD[0:16]		N*96-5		N*96-5	nsec
t_{dfCS}	RDn time to ACSn		-5		5	nsec
t_{drCS}	RDn time to ACSn	Word read	-5		5	nsec
		Byte read, even Waitcycles	N*96-5		N*96+5	nsec
t_{dfCS}	RDn time to CSx	CSx in Chip select mode	-5		5	nsec
t_{drCS}	RDn time to CSx	CSx in Chip select mode	N*96-10		N*96+10	nsec
t_{dfRC}	RDn time to RCSn		-5		5	nsec
t_{drRC}	RDn time to RCSn		-5		5	nsec
t_{dfRC}	RDN time to CSx	CSx in I/O exp mode	-5		10	nsec
t_{drRC}	RDn time to CSx	CSx in I/O exp mode	-5		10	nsec
t_{dsDA}	DAB[7:0] to RDn setup time				50	nsec
t_{dhDA}	RDn time to DAB[7:0] hold time		0			nsec

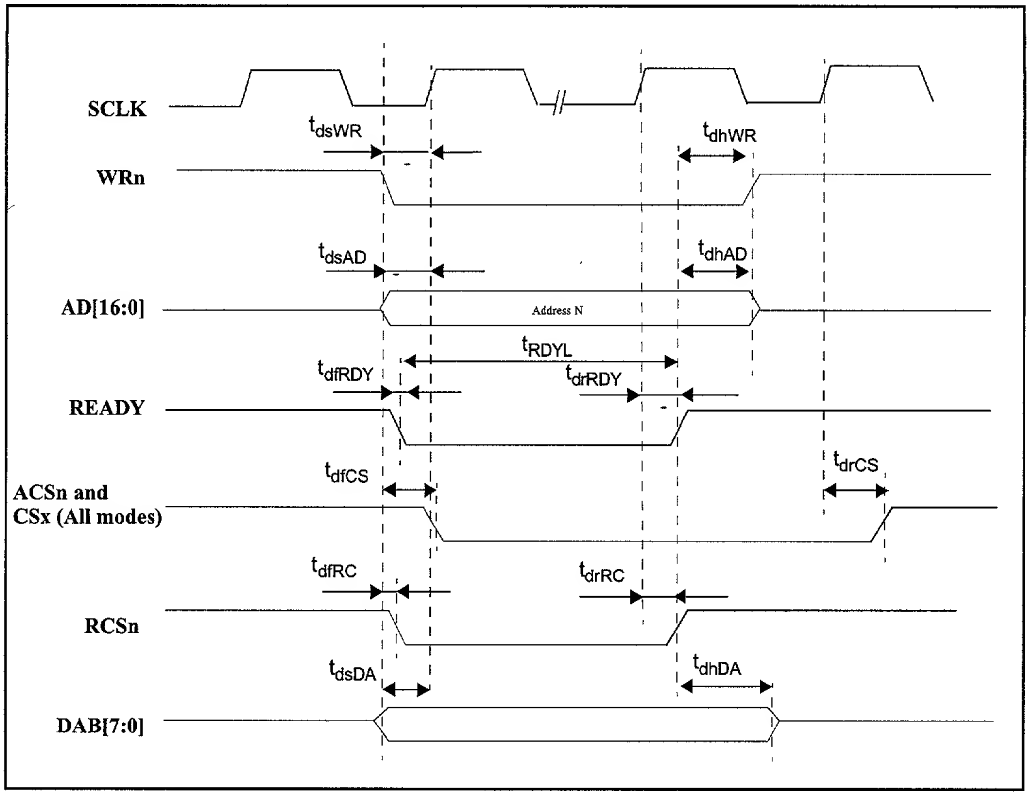


FIGURE 56. Write cycle timing diagram (HOLDn = '0')

Table 99: Timing characteristics for the SBI Interface write cycle (T=85°C, VDD = 2.7V, max. load = 30pF)

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
t_{dsWR}	WRN time to SCLK		55			nsec
t_{dhWR}	READY time to WRN				30	nsec
t_{dsAD}	AD[0:16] time to SCLK		55			nsec
t_{dhAD}	READY time to AD[0:16]				30	nsec
t_{dfRDY}	WRn time to READY				25	nsec
t_{drRDY}	SCLK time to READY		10			nsec
t_{RDYL}	READY Low period	Clock div. ratio N = 1 Clock div. ratio N>1	3N*96+30 N*96+30			nsec
t_{dfCS}	SCLK time to ACSn				5	nsec
t_{drCS}	SCLK time to ACSn				5	nsec
t_{dfCS}	SCLK time to CSx				15	nsec
t_{drCS}	SCLK time to CSx				15	nsec
t_{dsDA}	DAB[7:0] setup to SCLK		15			nsec
t_{dhDA}	READY to DAB[7:0] hold time		35			nsec

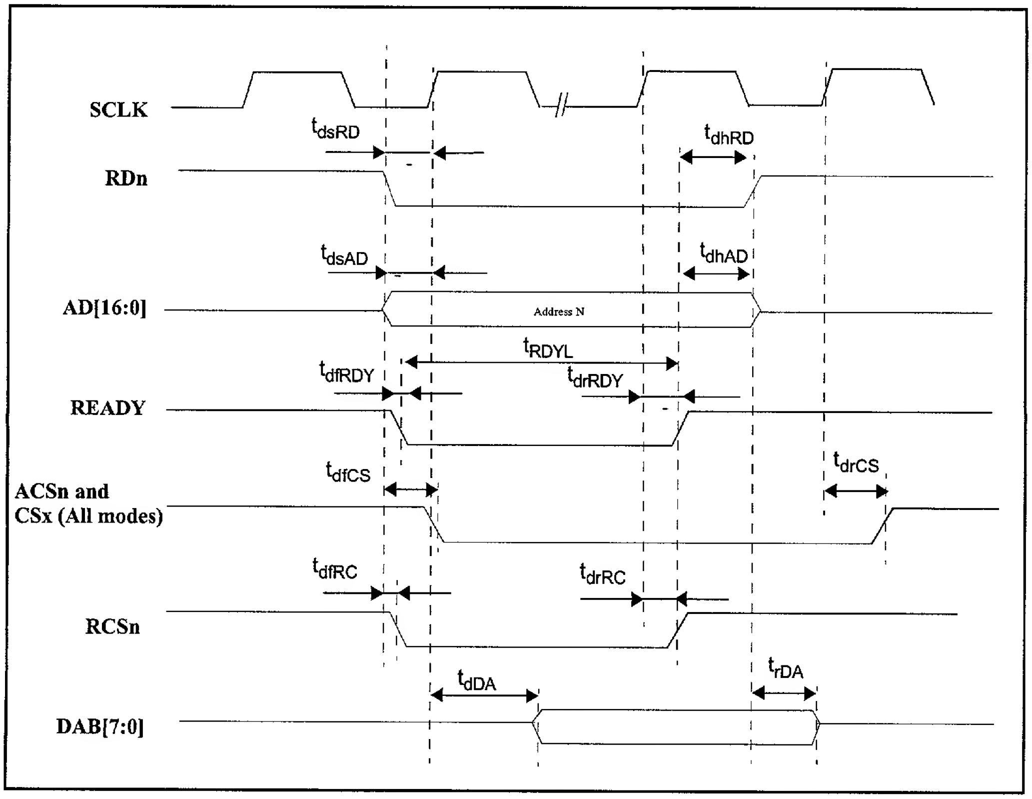


FIGURE 57. Read cycle timing diagram (HOLDn = '0')

Table 100:Timing characteristics for the SBI Interface read cycle (T=85°C, VDD = 2.7V, max. load = 30pF)

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
t_{dsRD}	RDN time to SCLK		55			nsec
t_{dhRD}	READY time to RDN				30	nsec
t_{dsAD}	AD[0:16] time to SCLK		55			nsec
t_{dhAD}	READY time to AD[0:16]				30	nsec
t_{dfRDY}	RDn time to READY				25	nsec
t_{drRDY}	SCLK time to READY		10			nsec
t_{RDYL}	READY Low period	Clock div. ratio N = 1 (Shared RAM) Clock div. ratio N = 2,3 (Shared RAM) Clock div. ratio N>3 Clock div. ratio N (other RAM)	4N*96+30 2N*96+30 N*96+30 N*96+30			nsec
t_{dfCS}	SCLK time to ACSn				5	nsec
t_{drCS}	SCLK time to ACSn				5	nsec
t_{dfCS}	SCLK time to CSx				15	nsec
t_{drCS}	SCLK time to CSx				15	nsec
t_{dDA}	SCLK to DAB[7:0]		370			nsec
t_{dhDA}	RDn to DAB[7:0] 3-state				15	nsec

5.4 AUDIO SPECIFICATIONS

Table 101:Microphone amplifier

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
V_{in_0dB}	Differential input voltage between MIC+ and MIC-	0dBm0 on COUT (Note 16) MIC-gain[3:0] = 0, @ 1020 Hz	134	158	182	mVrms
A	Gain	N * 2dB steps (N=1..15)	(N*2)-0.5	(N*2)	(N*2)+0.5	dB
R_{in}	Differential input impedance between MIC+ and MIC-		200			kΩ

Note 16: 0 dBm0 on COUT = -3.14 dB of max PCM value

Table 102:Microphone supply voltages

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
$\Delta(V_{REF+} - V_{REF-})$		I_{LOAD} = 0 mA	2.0	2.3	2.6	V
C_{load}	Differential load capacitance	see Figure 4.9	2.0			µF
R_{out}	Differential output resistance between VREF+ and VREF-			20	30	Ω
I_{load}	Differential output current				2	mA
Noise		CCITT weighted			-80	dBVp
PSRR	Power Supply Rejection Ratio		45			dB

Table 103:Loudspeaker output

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
V_{out_0dB}	Differential output voltage between LRS+ and LRS-	0dBm0 on CIN ((Note 17), LRS[3:0] = 3, @ 1020 Hz Load circuit A with $_{L1}$=1kΩ, C_{P1} as specified below or load circuit B with R_{L2}, C_{P2} and C_{Cs} as specified below	0.95	1.13	1.30	Vrms
A	gain	N * 1dB steps N=3,2,1,0,-1,...-12)	N - 0.5	N	N + 0.5	dB
R_{out}	Differential output impedance between LRS- and LRS+				20	Ω
C_{P1}	Load capacitance	see Figure 58 • $R_{L1} = \infty$ • $R_{L1} \leq 1$ kΩ			 30 100	 pF pF
R_{L1}	Load resistance		100			Ω

Table 103:Loudspeaker output

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
C_{P2}	Parallel load capacitance	see Figure 59			30	pF
C_{S2}	Serial load capacitance				30	µF
R_{L2}	Load resistance		600			Ω

Note 17: 0 dBm0 on CIN = -3.14 dB of max PCM value

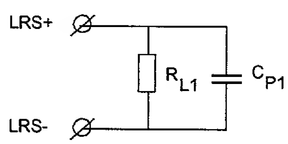


FIGURE 58. Load circuit A Dynamic loudspeaker

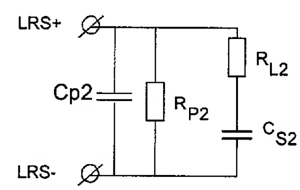


FIGURE 59. Load circuit B Piezo loudspeaker

Table 104:ADPCM gain setting

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
Gain adj.	ADPCM receiver output level	adjustment in steps of 3 dB	-36		0	dB
Sidetone	ADin to ADout	independent of gain adjustment, sidetone on.	-18		-12	dB

Table 105:CODEC characteristics

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
S/D_{AD}	Signal to total distortion ratio Analog/Digital	• see Figure 60, $R_{ab} = \infty$ • differential input signal between MIC+ and MIC- with f=1020Hz • ADPCM transcoder active • ECP in transparent mode • MICGAIN[3:0] = 0 1) 0 dBm0 on COUT 2) -40 dBm0 on COUT 3) -45 dBm0 on COUT	40 35 30	45		dB dB dB
S/D_{DA}	Signal to total distortion ratio Digital/Analog	• see Figure 60 • differential input signal between MIC+ and MIC- with f=1020Hz • ADPCM transcoder active • ECP in transparent mode • LRSGAIN[3:0] = 0 1) 0 dBm0 on CIN 2) -40 dBm0 on CIN 3) -45 dBm0 on CIN	40 35 30	50		dB dB dB
$NOISE_{AD}$	Idle channel noise Analog/ Digital	• see Figure 60, R_{ab} = 0 Ohm • Relative to 0 dBm0 • MICGAIN[3:0] = $0F_{16}$		-80	-70	dBmp
$NOISE_{DA}$	Idle channel noise Digital/ Analog	• see Figure 60 • Relative to 0 dBm0 • LRSGAIN[7:4] = 0		-83	-80	dBmp
$PSRR_{AD}$	Power supply rejection ratio Analog/Digital	• See Figure 60, AVD2 to COUT, f = 100 Hz to 4 kHz • MICGAIN[3:0] = 0 • MICGAIN[3:0] = $0F_{16}$	40 50			dB dB
$PSRR_{DA}$	Power supply rejection ratio Digital/Analog	• See Figure 60, AVD2 to LRS+/-, f = 100 Hz to 4 kHz • LRSatt[7:4] = 0	45			dB
$PSRR_{VREF}$	Power supply rejection Vref output	• See Figure 60, AVD2 to Vref+/-, f = 100 Hz to 4 kHz	45			dB
FREQ. RESP. AD	Frequency response Analog/ Digital	• see measurement diagram Figure 60, $R_{ab} = \infty$ • relative to 1020 Hz	see frequency response diagram Figure 61			
FREQ. RESP. DA	Frequency response Digital/Analog	• see measurement diagram Figure 60, R_{ab} = 1 kOhm • relative to 1020 Hz	see frequency response diagram Figure 62			

Note 18: All noise and distortion measurements are done with CCITT weighted signals. 0 dBm0 on COUT and CIN = -3.14 dB of max. PCM value